Service Manual Level 3
for
BenQ mobile
EF51

Release	Date	Department	Notes to change
R 1.0	26.08.2006	ISC S CES	New document

Table of Content

1 Introduction

1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3-4.

1.2 Scope

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Siemens mobile phones up to level 3.

1.3 Terms and Abbreviations

2 List of available level 3 parts

Produkt	Ordre Number	Description CM
EF51	L50610-B6217-D670	IC CMOS MC74VHC1G32DFT1 M580/S88/EF51
EF51	L50610-B6238-D670	IC CMOS SN74LVC1T45DCKR SC70 S88/EF51
EF51	L50610-B6258-D670	IC CMOS NL17SZ08DFT2G SC70 EF51
EF51	L50610-B6259-D670	IC CMOS NL17SZ86DFT2G SC70-5 EF51
EF51	L50610-B6261-D670	IC CMOS SN74AVC20T245ZQLR PBGA EF51
EF51	L50610-C6287-D670	IC ANALOG SW NC7S M580/S88/EF51/CF61
EF51	L50610-C6288-D670	IC DC CONV LM3501TLX TL08A 8P M580/E61/EF51/CF61
EF51	L50610-C6289-D670	IC VR MAS9124A2GC06 TSOT-5 M580/S88/CL71/E61/EF51/
EF51	L50610-C6290-D670	IC VR MIC5213-2.8YC5 SC70 M580/S88/EF51/CF61
EF51	L50610-C6388-D670	IC ANA CXG1180EQ S88/CL71/EF51
EF51	L50610-C6390-D670	IC ANA TPA2010D1YZ S88/CL71/E61/EF51/CF61
EF51	L50610-C6392-D670	IC ANA NUF2221W1T2 S88/E61/EF51/CF61
EF51	L50610-C6394-D670	IC ANA BH6053GU S88/E61/EF51
EF51	L50610-C6395-D670	IC ANA ISL6292CCR3 S88/CL71/E61/EF51/CF61
EF51	L50610-C6425-D670	IC PWR AMPSKY77328 6*6*1.2 20P
EF51	L50610-C6439-D670	IC VR R5323N032B-TR-F SOT23-6 EF51
EF51	L50610-F6483-D670	IC FLASH M6MGA157F S88/EF51
EF51	L50610-G6322-D670	IC CPU SH7327-DH6417327 BGA256
EF51	L50610-U6243-D670	IC INTF TWL3025BZGMR PBGA 100P M580/S88/CL71/E61/E
EF51	L50610-U6244-D670	IC IR XCVR HD155165BPEB M580/S88/CL71/E61/EF51
EF51	L50610-U6268-D670	IC BC313141A07-IXF S88/EF51/CF61
EF51	L50610-U6294-D670	IC DETECTOR XC61GC2502HRN USP3 EF51
EF51	L50610-U6295-D670	IC HALL-EFF SW A3212ELHLT-T 3P EF51
EF51	L50610-U6296-D670	IC AUDIO DAC WM8753LGEB-RVBGA EF51
EF51	L50610-U6297-D670	IC RECV TEA5767HN HVQFN 40P
EF51	L50622-F4103-K	THERMISTOR NTC 10K 0402 NTH5G M580/S88/CL71/E61/EF
EF51	L50630-C1187-D670	FET MOS FDC6506P M580/S88/E61/EF51/CF61
EF51	L50630-C1198-D670	DISTRANS FDG6303N S88/E61/EF51/CF61
EF51	L50630-C1207-D670	FET MOS NTE4151PT1G PC SC-89 EF51
EF51	L50634-Z97-C553	JACK DC PWR PA05302-QNJ M580/S88/E61/CL71/EF51
EF51	L50634-Z97-C554	CONN ANT 5.1 3 5 RF05301-PG M580/S88/CL71/EF51/CF6
EF51	L50634-Z97-C558	CONN I/O 10P P0.5 215+916+2941 M580/S88/E61/CL71/M
EF51	L50634-Z97-C559	CONN MIC 2P TRA21-2K8 56F55 M580/EF51
EF51	L50634-Z97-C564	CONN SPK1A-2K0710 3.6*7.7 M580/EF51/CF61
EF51	L50634-Z97-C637	Connector SIM BM05306-D S88/EF51/E61
EF51	L50634-Z97-C796	CONN SKT 24P D0.4 H1.2 BF4-011 EF51
EF51	L50634-Z97-C797	CONN FPC 31P RT D0.3 HRS/FH23 EF51
EF51	L50634-Z97-C798	CONN BATT 3P D2.5 AB303M-20G1G EF51
EF51	L50634-Z97-C799	CONN BTB 1.5S_N18P14.3*6.9*2.5 EF51/CF61
EF51	L50634-Z97-C800	CONN SD MINI 11PD1.3 MLX/50052 EF51
EF51	L50634-Z97-C801	CONN VOLUM KEY 10.2*1.7*2.8 5P EF51/CF61
EF51	L50640-C2135-D670	XTOR MUN5235DW1T1G SOT-363 EF51
EF51	L50640-C2143-D670	XTOR BC807-40W M580/S88/E61/EF51/CF61

EF51	L50640-D110-D670	TVS 6.5V170P 0402 M580/S88/E61/EF51/CF61
EF51	L50640-D118-D670	DISDIODE TVS TVM0A S88/EF51/CF61
EF51	L50640-D119-D670	DISDIODE TVS SFI05 S88/E61/EF51/CF61
EF51	L50640-D123-D670	DISDIODE UCLAMP 05 S88/EF51
EF51	L50640-D124-D670	DISDIODE VAR HVD35 S88/CL71/E61/EF51
EF51	L50640-D133-D670	DIODE VAR CAP BB202 SOD-523 EF51
EF51	L50640-D134-D670	TVS 5.5V 80P 0402 TVM0A110M800 EF51
EF51	L50640-D135-D670	TVS 15V150PF0603 TVM1A150L151R EF51
EF51	L50640-D3142-D670	DIODE ZEN 6.06-6.33V 200MW UMD M580/S88/E61/EF51/C
EF51	L50640-D5110-D670	DIODE SB 0.2A30V M580/S88/CL71/E61/EF51/CF61
EF51	L50640-D5121-D670	DISDIODE ARR DAN22 S88/E61/EF51/CF61
EF51	L50640-D5123-D670	DISDIODE RB161M-20 S88/E61/EF51/CF61
EF51	L50640-D5124-D670	DISDIODE PMEG2020E S88/CL71/E61/EF51/CF61
EF51	L50640-D5125-D670	DISDIODE 1PS79SB30 S88/CL71/E61/EF51
EF51	L50640-D5126-D670	DISDIODE PMEG2005E S88/EF51/CF61
EF51	L50640-L2188-D670	LED WHITE LTW-C192TL5 1.6*0.8 EF51
EF51	L50645-F102-Y48	XTAL 26MHZ 10PF 8PPM U-860-1-1 M580/S88/E61/EF51
EF51	L50645-F102-Y49	XTAL 32.768 K12.5PF20PPM M580/S88/CL71/E61/EF51/CF
EF51	L50645-F102-Y69	XTAL 30MHZ 8PF 30PPM DSX221S EF51
EF51	L50645-G200-Y30	OSC 48MHZ 15PF 50PPM DS0221SV EF51
EF51	L50645-J4683-Y34	IC ASIC D751992AZH S88/CL71/E61/EF51/CF61
EF51	L50645-K280-Y420	FILSAW 1842.5MHZ SAFEH1G S80/S82/SFG75/M220/S77/S8
EF51	L50645-K280-Y421	FILTER SAW 942.5M SAFEH942MFN S80/S82/SFG75/S77/S8
EF51	L50645-K280-Y425	FILTER BAND 2.45GHZ LFB M580/S88/CL71/EF51/CF61
EF51	L50645-K280-Y437	FILTER SAW 1960MHZ SAFEH1G96FB M220/S88/CL71/E61/E
EF51	L50645-K280-Y453	FIL LFA24-2A1A144M S88/E61/CF61
EF51	L50664-F6101-J2	CAP ARRAY 100PF 50V 8P K0805S NPO EF51
EF51	L50664-F6106-M	CAP ARRAY 1U 10V 4P M 0504 EF51
EF51	L50664-F6220-K	CAP ARRAY 22P 50V J0805S NPO M580/S88/E61/EF51

3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- SW-Update-Cable TI-Platform (M315/M580/S88...) F30032-P601-A1
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

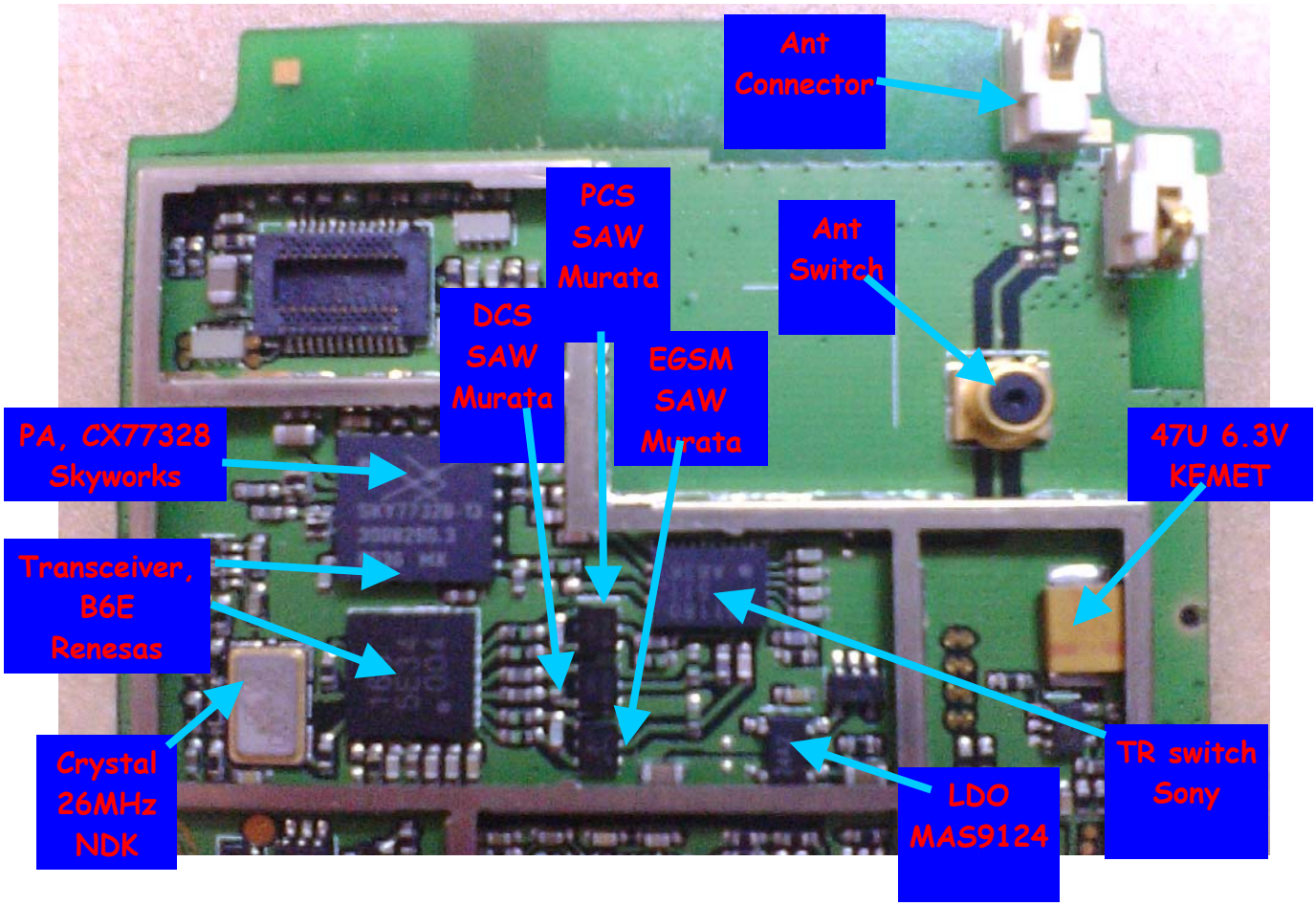
Reference: Equipment recommendation V1.6
(downloadable from the technical support page)

4 Required Software for Level 3

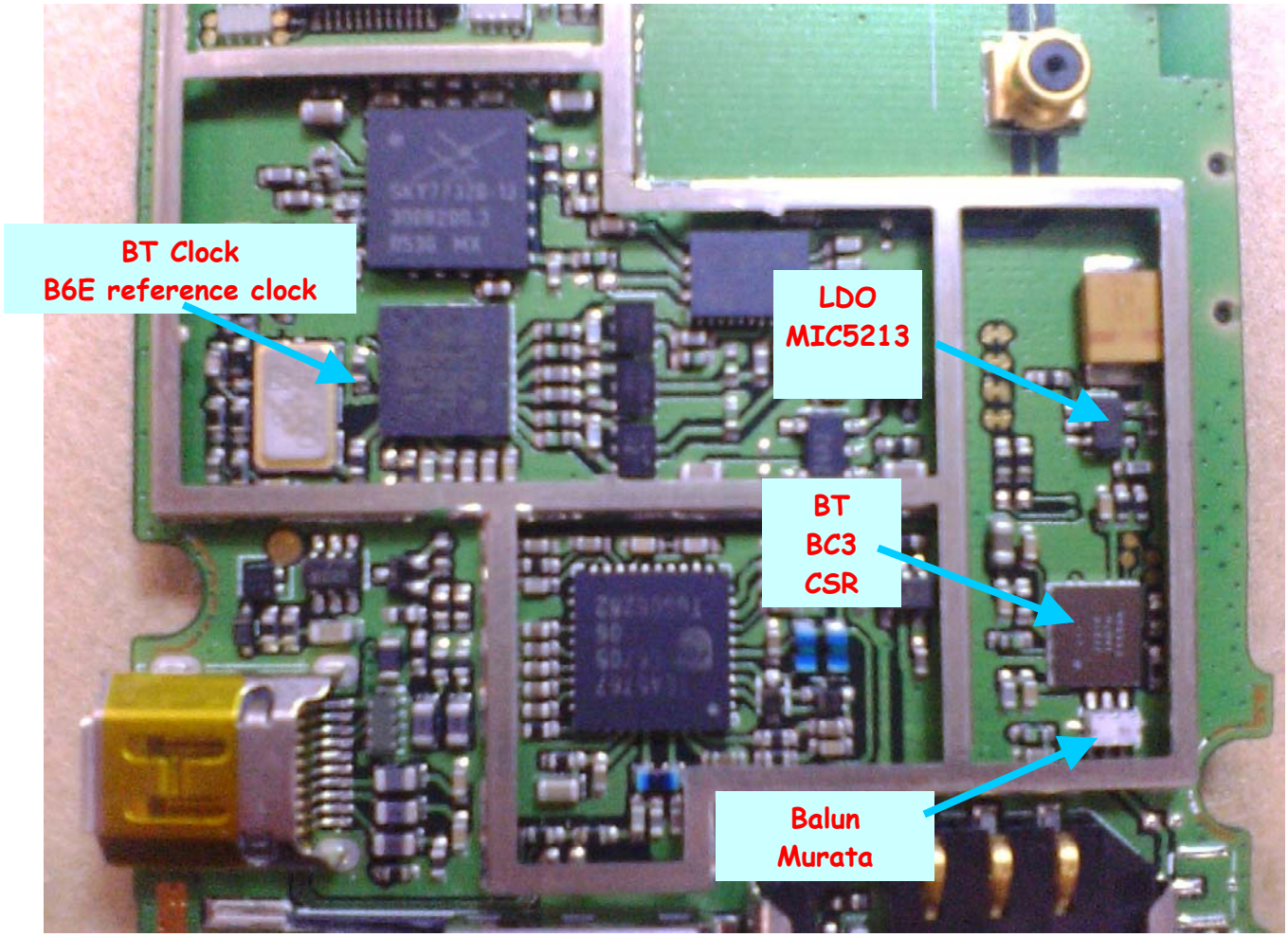
- Windows XP
- XCSD Tool 1.5.5 higher
- GRT Version 3 or higher
- Internet unblocking solution (JPICS)

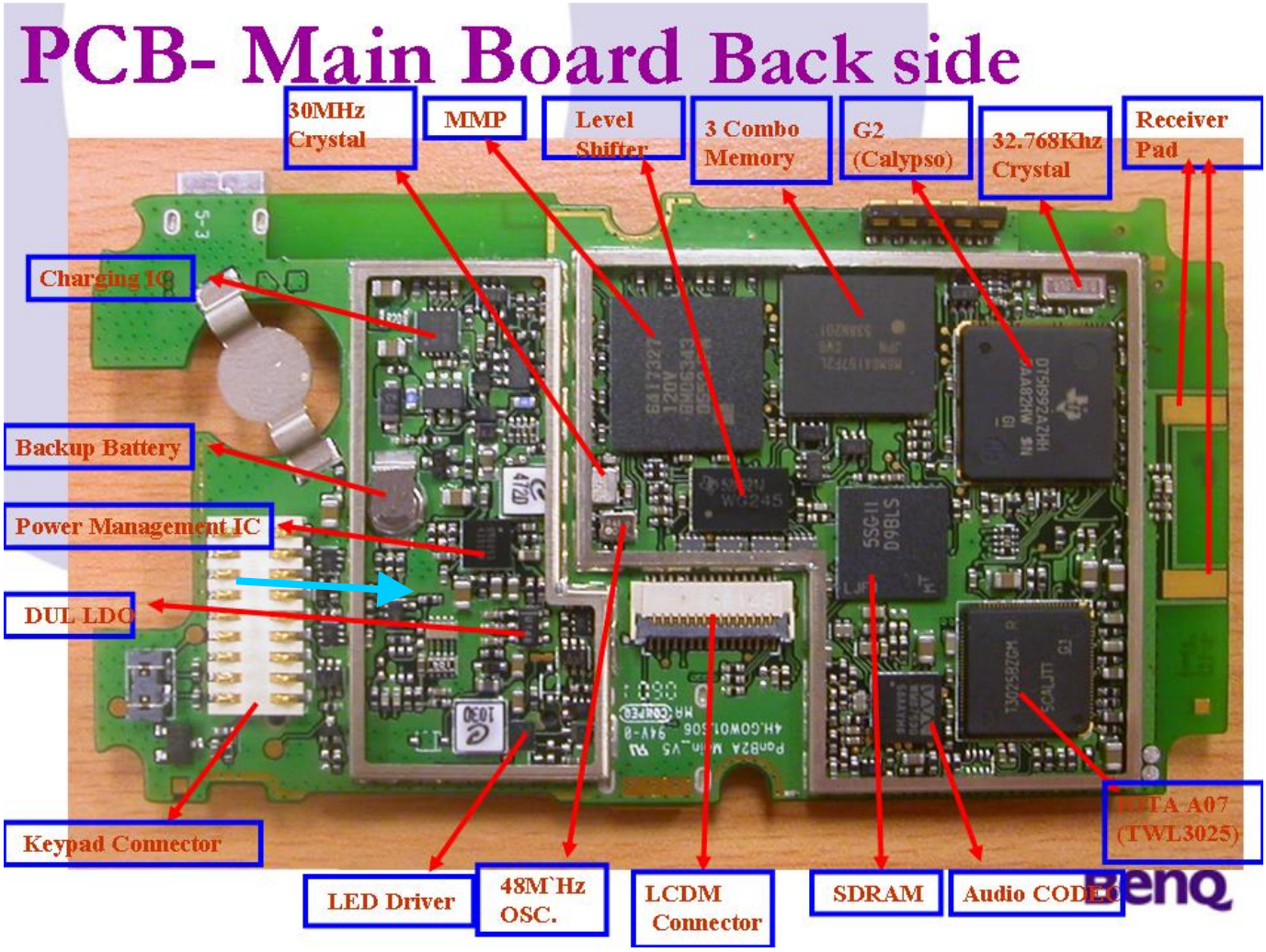
PCB Main Board Overview

PanB2A RF Component & Placement



PanB2A BT Component & Placement





5 Radio Part

The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

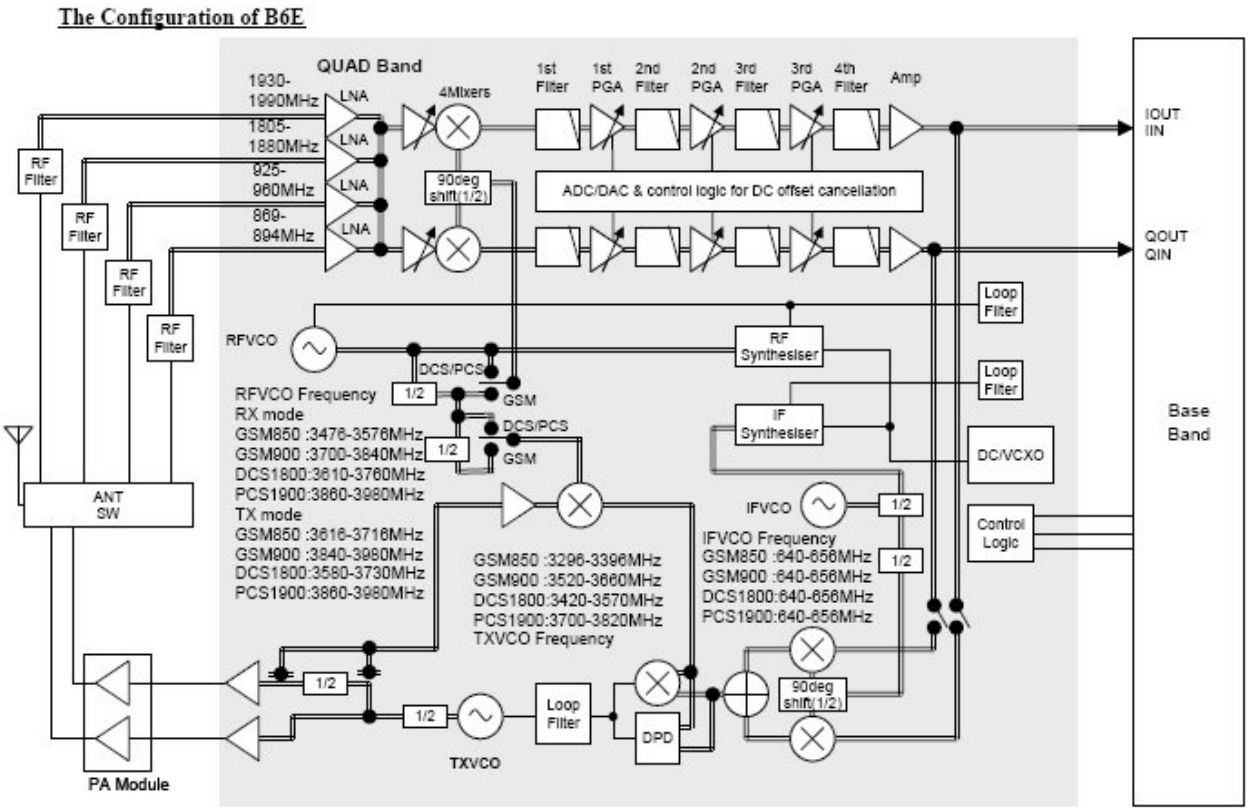
Transmitter and Receiver are never active at the same time. Simultaneous receiving in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible. Simultaneous transmission in the GSM850/EGSM900 and GSM1800/GSM1900 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

EF51 RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000) supporting GPRS functionality up to multiclass 10.

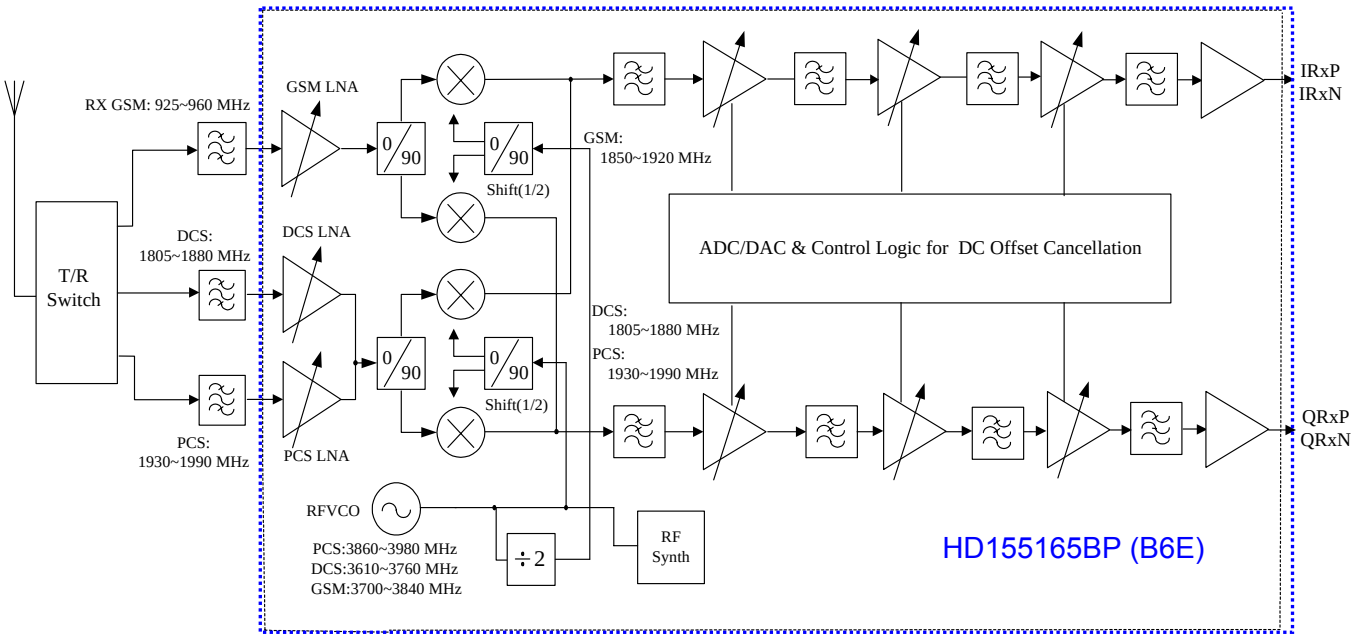
The RF-circuit consists of the following components:

- Renesas Bright 5PL chip set (HD155153NP) with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2 (without loop filter)
  - Integrated TxVCO (without loop filter and core inductors for GSM)
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - Active part of 26 MHz reference oscillator
  - Integrated Polar Loop, phase and amplitude control of transmitted output power
- Renesas LTCC transmit PA PF09026B (incl. integrated power control circuitry for GMSK mode)
- Frontend-Module including RX-/TX-switch and EGSM900 / DCS1800 / PCS 1900 receiver SAW-filters
- Crystal and passive circuitry of the 26MHz VCXO reference oscillator

5.1 Block diagram RF part



5.2 Receiver Operation

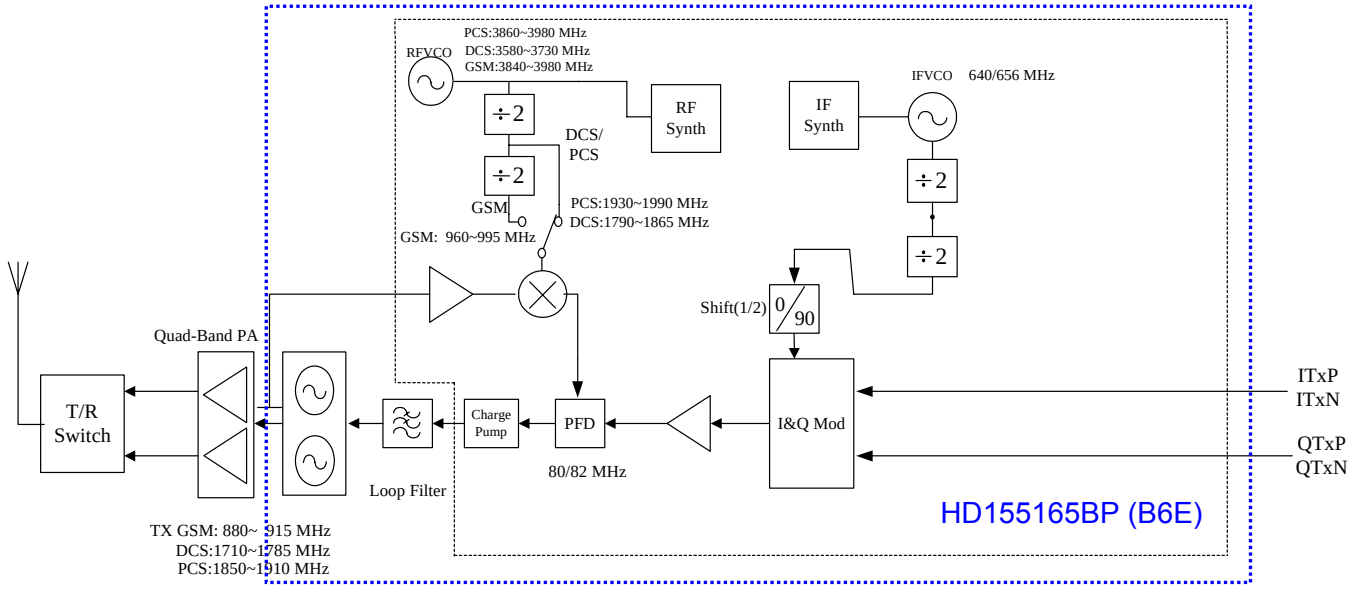


The HD155165BP receiver is based upon the HD155155NP direct conversion design. As HD155165BP supports quad band, the front end incorporates four LNAs and mixers. The incoming RF signals are mixed directly down to I/Q base-band by the front-end block. This incorporates four LNAs / four buffers and Gilbert Cell mixer blocks optimized for operation at 850MHz, 900MHz, 1800MHz, 1900MHz respectively.

The front-end block is followed by two closely matched base-band amplifier chains. These include distributed low pass filter, three switched gain stages and one fixed gain stage. In addition, the base-band section integrates A/D and D/A converters which provide automatic on-chip correction of DC offsets. The three switched gain stages in each channel are DC coupled and provide 90dB gain control range with 2dB step size. The first PGA has a voltage gain range (x8-x1) with 6dB steps. The second PGA has a gain range (x8-x0.125) with 2dB steps. The third PGA has a gain range (x8-x0.125) with 2dB steps. The final fixed gain amplifier provides a gain of x3 or x6. The gain is set to match the on-chip levels to the input dynamic range of the base-band. The base-band filtering in each channel comprises a single RC low pass filter at the input of the first switched gain stage and three 2nd order Butterworth filters, one at the input of each of the other switched gain stages. The R/C filter requires an off-chip capacitor for each channel. The Butterworth filters are fully integrated on-chip.

The base-band PGA includes a DC offset cancellation system. The auto calibration system uses a successive approximation technique and requires around 20us to perform a three stages calibration. The system calibrates out the offsets arising in both I and Q receives channels.

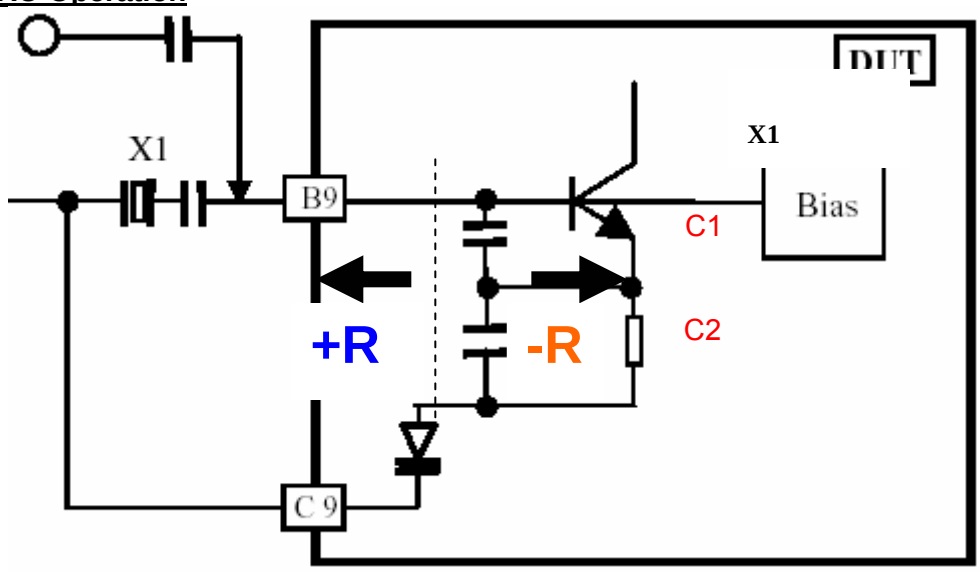
5.3 Transmitter Operation



The B6E generates a modulated signal at IF with a quadrature modulator and converts it to final frequency with an Offset Phase Locked Loop (OPLL).
The Offset Phase Locked Loop is simply a PLL with a down conversion mixer in the feedback path. Using a down converter in the feedback path acts as an up-converter in the forward path. This allows the output frequency to be different from the comparison frequency without affecting the normal operation of the loop. Phase/frequency changes in the reference signal are not scaled, as they would be if a divider were used in the feedback path, hence the modulation is faithfully reproduced at the final frequency.
The main advantage of the OPLL in this application is that it forms a tracking band pass filter around the modulated signal. This is because the loop cannot respond to phase variations at the reference that are outside its closed loop bandwidth. Thus the broad band phase noise from the quadrature modulator is shaped by the frequency response of the closed loop allowing the TX noise specification to be met without further filtering.
A secondary advantage of the OPLL is that the output signal, coming from a VCO, is truly constant envelope. This removes the problem of spectral spreading caused by AM to AM and AM to PM conversion in the power amplifier.
The OPLL is formed from an on chip Gilbert cell down converter, limiter and phase detector with on chip passive loop filter. The phase detector is implemented as a Gilvert cell with current source output stage. The current output allows an integrator to be included in the passive loop filter. This is similar to the technique commonly used in PLL synthesizers. A digital phase detector is used to speed OPLL locking. After locking, the digital phase detector is switched off and the analogue phase detector becomes active.

5.4 Frequency generation

DCXO Operation



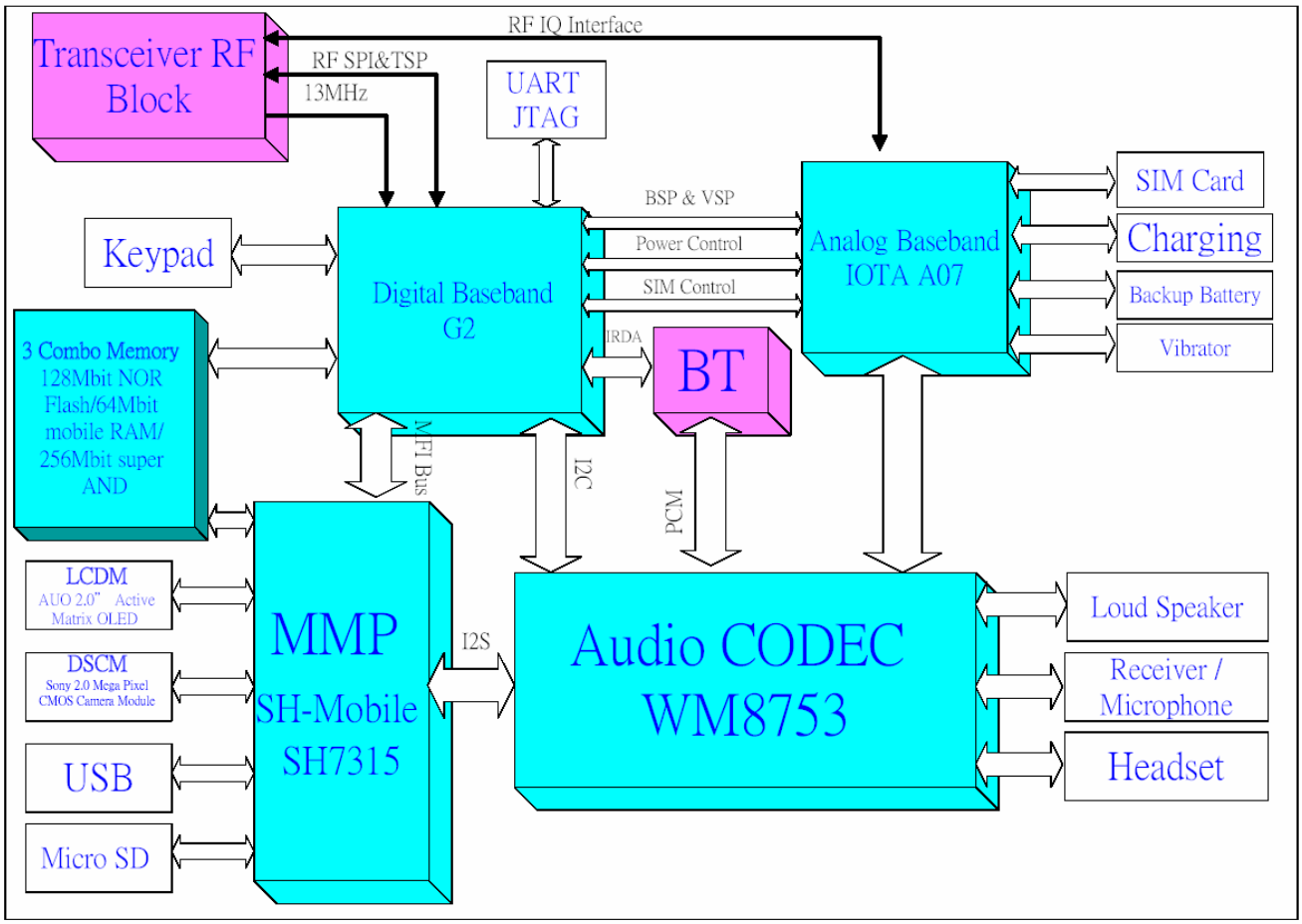
HD155165BP provides a DCXO function. With that function, we can build a reference clock generation circuits as shown in the above graph. This means that the VCTCXO module is not necessary for clock application, and only one crystal with 8ppm tolerance and one varactor are enough.
The transistor in HD155165BP and two internal capacitors (C1, C2) provide a negative resistance, and the crystal (X1) combined with some other passive components to provide a positive resistance. When these two resistance values equal to each other at some frequency, the oscillation will happen at that frequency. In our design target, the oscillation frequency should be within 26MHz +/-15 ppm at least.

6 Logic / Control

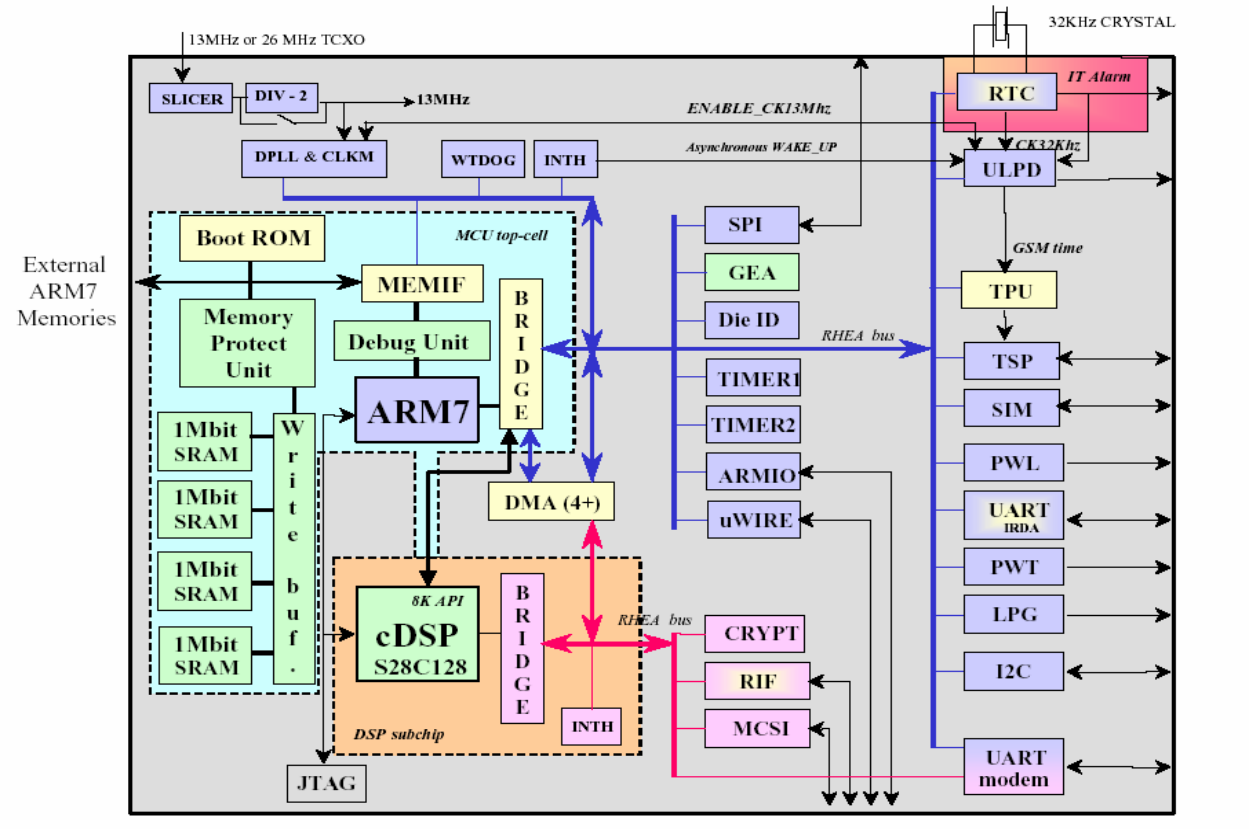
6.1 Overview Hardware Structure

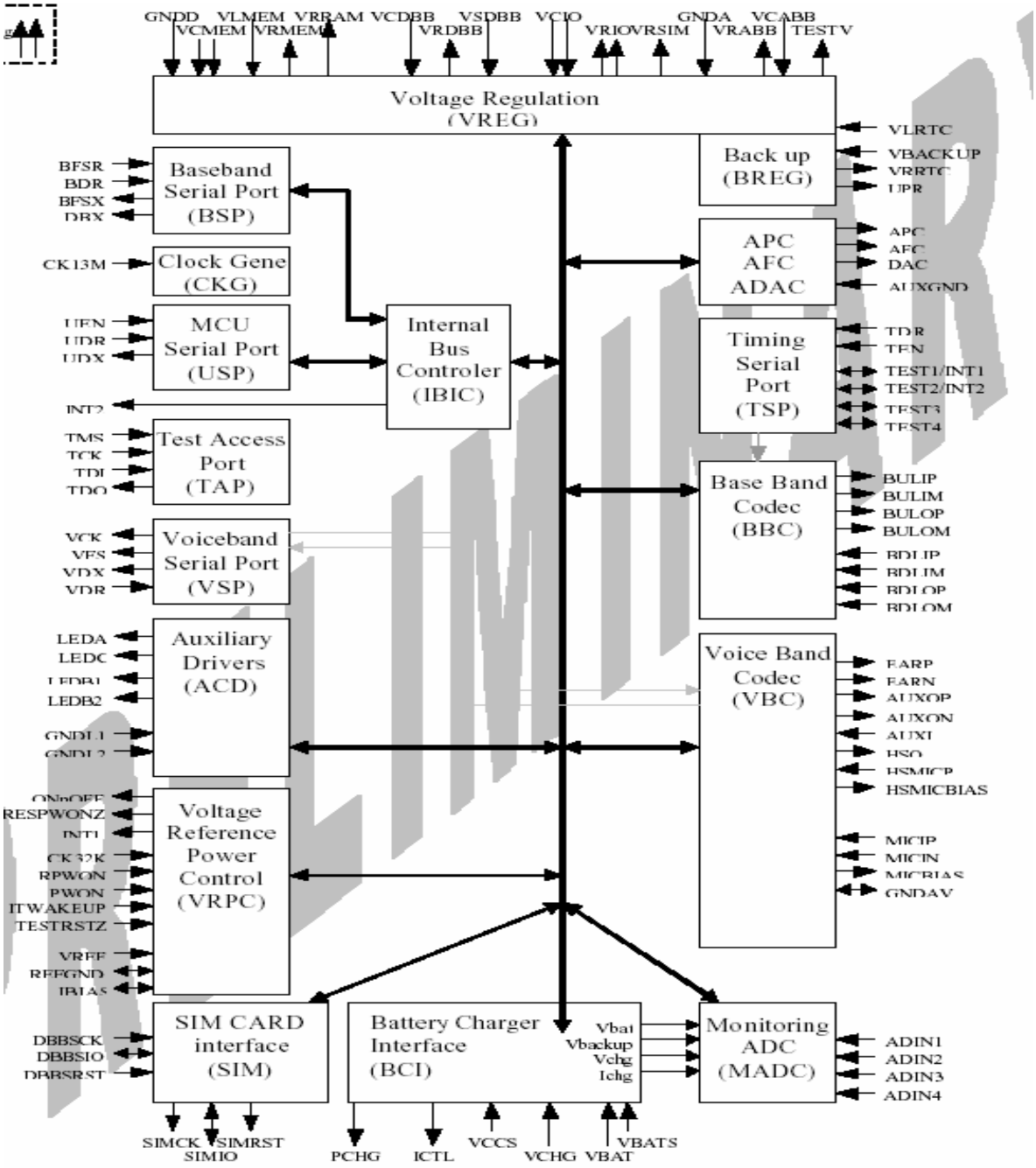
Introduction:
Pandora B2 utilizes TI's chipsets (CALYPSO and IOTA) and RENESAS's chipset (SHJ2SL) as base-band solution. Base-band is composed with three potions: Logic, Analog/Codec and MMP. CALYPSO is a GSM/GPRS digital base-band logic solution included microprocessor, DSP, and peripherals. IOTA is a combination of analog/codec solution and power management which contain base-band codec, voice-band codec, several voltage regulators and SIM level shifter etc. SHJ2SL is a multimedia solution included microprocessor, DSP, internal memory, and interrupt controller. In addition, Pandora B2 integrates with other features such as CMOS DSC module, Mini-SD card, vibration, melody and charging etc. The following sections will present the operation theory with circuitry and descriptions respectively.

6.2 Block Diagram



6.3 CALYPSO (HERCROM400)





6.4 Calypso

CALYPSO (HERCROM400) is a chip implementing the digital base-band processor of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE) and an internal 4M-bit RAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.

Major functions of this chip are as follows:

6.4.1 Real Time Clock (RTC)

The RTC block is an embedded RTC module fed with an external 32.768KHz Crystal. Its basic functions are:

1. Time information (seconds/minutes/hours)
2. Calendar information (Day/Month/Year/ Day of the week) up to year 2099
3. Alarm function with interrupts (RTCINT is generated to wake up ABB)
4. 32KHz oscillator frequency gauging

6.4.2 Pulse Width Light (PWL)

This module allows the control of the backlight of LCD and keypad by employing a 4096 bit random sequence.

6.4.3 MODEM-UART

This UART interface is compatible with the NS 16C750 device which is devoted to the connection to a MODEM through a standard wired interface. The module integrates two 64 words (9 and 11 bits) receive and transmit FIFOs which trigger levels are programmable. All modem operations are controllable either via a software interface or using hardware flow control signals. In Hyperion B1, we implement software flow control by only two signals: TXD and RXD.

6.4.4 I2C master serial interface (I2C)

The I2C (Philips standard) is a half-duplex serial port using 2 lines (data and clock) for data transmission with software addressable external devices. In Hyperion B1, we employ I2C bus to control CLI in Audio Codec.

The I2C signals are defined as follows:

I2C_SCL: programmed to the fast transmission mode (400KHz)

I2C_SDA: the serial bi-directional data of the Audio Codec controller

6.4.5 General Purposes I/O (GPIO)

Calypso provides 16 GPIOs configurable in read or write mode by internal registers. In Hyperion B1, we utilize all of them as follows:

IO0: Let MMP power-on reset; 'Low active'
IO1: Enable LCD back light; 'H': enable, 'L': disable
IO2: Control MMP's MFI mode; 'H': 68-type mode, 'L': 80-type mode
IO3: Hall sensor INT
IO4: Hall sensor status; 'L': close, 'H': open
IO5: SIM power control
IO6: Accessory detect; 'H': no accessory, 'L': accessory in
IO7: Reset of external device: For Pandora B2, Reset for 3 combo memory and LCD
IO8: Indicates whether MMP is in software standby mode
IO9: I2C clock signal for FM
IO10: Detection of Mini-SD card; 'H': No plugged in, 'L': plugged in
IO11: BT power enable
IO12: I2C data signal for FM
IO13: INT request for MMP
IO14: SRAM high-byte enable
IO15: SRAM low-byte enable

6.4.6 Serial Port Interface (SPI)

The SPI is a full-duplex serial port configurable from 1 to 32 bits and provides 3 enable signals programmable either as positive or negative edge or level sensitive. This interface is working on 13MHz and is used for the GSM/GPRS baseband and voice A/D, D/A with IOTA

6.4.7 Memory Interface and internal Static RAM

For external memory device (Flash and SRAM), this interface performs read and write access with adaptation to the memory width. It also provides 6 chip-select signals corresponding each to an address range of 8 mega bytes. One of these chip-select is dedicated to the selection of an internal memory. In Hyperion B1, we employ nCS0/nCS1 (nCS0_NROM/nCS1_NROM) for external Flash and nCS2 (nCS2_NSRAM) for external SRAM.

A 4Mbit SRAM is embedded on the die and memory mapped on the chip-select nCS6 of the memory interface.

6.4.8 SIM Interface

The Subscriber Identity Module interface will be fully compliant with the GSM 11.11 and ISO/IEC 7816-3 standards. Its external interface is 3 Volts only. 5 Volts adaptation will be based on external level shifters.

6.4.10 Time Serial Port (TSP)

The TPU is a real-time sequencer dedicated to the monitoring of GSM/GPRS baseband processing. The TSP is a peripheral of the TPU which includes both a serial port (32 bits) and a parallel interface. The serial port can be programmed by the TPU with a time accuracy of the quarter of GSM bit. The serial port is uni-directional (transmit only) when used with IOTA. The serial port provides 4 enable signals programmable either as positive or negative edge or level sensitive. This serial port is derived from 6.5MHz and used to control the real time GSM windows for the baseband codec and the windows for ADC conversion

6.5 IOTA

Together with a digital base-band device (Calypso), IOTA is part of a TI DSP solution intended for digital cellular telephone applications including GSM 900, DCS 1800 and PCS 1900 standards (dual band capability).

It includes a complete set of base-band functions to perform the interface and processing of voice signals, base-band in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis. IOTA interfaces with the digital base-band device through a set of digital interfaces dedicated to the main functions of CALYPSO, a base-band serial port (BSP) and a voice-band serial port (VSP) to communicate with the DSP core (LEAD), a micro-controller serial port to communicate with the micro-controller core and a time serial port (TSP) to communicate with the time processing unit (TPU) for real time control.
IOTA includes also on chip voltage reference, under voltage detection and power-on reset circuits.

Major functions of this chip are as follows:

6.5.1 Baseband Codec (BBC)

The baseband codec includes a two-channel uplink path and a two-channel downlink path. The baseband uplink path (BUL) modulates the bursts of data coming from the DSP via the baseband serial port (BSP) and to be transmitted at the antenna. Modulation is performed by a GMSK modulator. The GMSK modulator implemented in digital technique generates In-phase (I) and Quadrature (Q) components, which are converted into analog base-band by two 10 bits DACs filters. It also includes secondary functions such as DC offset calibration and I/Q gain unbalance.

The baseband downlink path (BDL) converts the baseband analog I & Q components coming from the RF receiver into digital samples and filters these resulting signals through a digital FIR to isolate the desired data from the adjacent channels. During reception of burst I & Q digital data are sent to the DSP via the baseband serial port (BSP) at a rate of 270 KHz.

6.5.2 Automatic Frequency control (AFC)

The automatic frequency control function consists of a digital to analog converter optimized for high resolution DC conversion. Its purpose is to control the frequency of the GSM 13MHz oscillator to maintain mobile synchronization on the base station and allow proper transmission and demodulation.

6.5.3 Automatic Power Control (APC)

Purpose of the Automatic Power Control (APC) is to generate an envelope signal to control the power ramping up, ramping down and power level of the radio burst.

The APC structure is intended to support single slot and multi-slots transmission with smooth power transition when consecutive bursts are transmitted at different power level. It includes a DAC and a RAM in which the shape of the edges (ramp-up and ramp-down) of the envelope signals are stored digitally. This envelope signal is converted to analog by a 10 bits digital to analog converter. Timing of the APC is generated internally and depends of the real time signals coming from the TSP and the content of two registers which control the relative position of the envelope signal versus the modulated I & Q.

6.5.4 Time serial port (TSP)

Purpose of the time serial port is to control in real time the radio activation windows of IOTA which are BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration and BDL receive and the ADC conversion start.

These real time control signals are processed by the TPU of DBB and transmitted serially to ABB via the TSP, which consists in a very simple two pins serial port. One pin is an enable (TEN) the other one the data receive (TDR). The master clock CK13M divided by 2 (6.5MHz) is used as clock for this serial port.

6.5.5 Voice band Codec (VBC)

The VBC processes analog audio components in the uplink path and transmits this signal to DSP speech coder through the voice serial port (VSP). In the downlink path the VBC converts the digital samples of speech data received from the DSP via the voice serial port into analog audio signal. Additional functions such as programmable gain, volume control and side-tone are performed into the voice band codec.

6.5.6 Micro-controller serial port (USP)

The micro-controller serial port is a standard synchronous serial port. It consists in three terminals, data transmit (UDX), data receive (UDR) and port enable (UEN). The clock signal is 13MHz clock. The USP receives and sends data in serial mode from and to the external micro-controller and in parallel mode from and to the internal GSM Baseband a Voice A/D D/A modules. The micro-controller serial port allow read and write access of all internal registers under the arbitration of the internal bus controller.

6.5.7 SIM card shifters (SIMS)

The SIM card digital interface in ABB insures the translation of logic levels between DBB and SIM card, for transmission of 3 different signals; a clock derived from a clock elaborated in DBB, to the SIM card (DBBSCK➔SIMCLK). a reset signal from DBB to the SIM card (DBBSRST➔SIMRST), and serial data from DBB to SIM card (DBBSIO➔SIMIO) and vice-vera.

The SIM card interface can be programmed to drive a 1.8V and 3 V SIM card

6.5.8 Voltage Regulation (VREG)

Linear regulation is performed by several low dropout (LDO) regulators to supply analog and digital baseband circuits.

(1) LDO VRDBB generates the supply voltage (1.8V, 1.5V,and 1.2V) for the digital core of DBB. In Hyperion B1, it is programmed to 1.5V. This regulator takes power from the battery voltage.
(2) LDO VRABB generates the supply voltage 2.8V for the analog function of ABB. It is supplied by the battery.
(3) LDO VRIO generates the supply voltage 2.8V for the digital core of ABB and digital I/O's of DBB and ABB. It is supplied from battery voltage.
(4) LDO VRMEM generates the supply voltages 2.8V for DBB memory interfaces I/O's.
(5) LDO VRRAM generates the supply voltages 2.8V for DBB memory interfaces I/O's.
(6) LDO VRRTC generates the supply voltages (1.8,1.5, or 1.2V) and supply voltage 1.5V for the following block of DBB (real time clock and 32K oscillator). It's supplied by UPR.
(7) LDO VRSIM generates the supply voltages (1.8V, 2.9V) for SIM card interface I/O's.

6.5.9 Baseband Serial Port (BSP)

The BSP serial interface is used for both configuration of the GSM baseband and voice A/D D/A (read and write operation in the internal registers), and transmission of the radio data to the DSP during reception of a burst by the downlink part of the GSM baseband & voice A/D D/A. Four pins are used by the serial port: BFSR and BDR for receive, BFSX and BDX for transmit. BDX is the transmitted serial data output. BFSX is the transmit frame synchronization and is used to initiate the transfer of the transmit data. BDR is the received serial input. BFSR is the receive frame synchronization and is used to initiate the reception data.

6.5.10 Battery charger Interface (BCI)

The main function of the ABB charger interface is the charging control of either a 1-cell Li-ion Battery or 3-serie Ni-MH cell batteries with the support of the micro-controller. The battery monitoring uses the 10 bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage. The magnitude of the charging current is set by the 10 bits of a programming register converted by an 10 bit Digital to Analog Converter, whose output sets the reference input of the charging current control loop. The battery charger interface performs also some auxiliary functions. They are battery pre-charge, battery trickle charge and back-up battery charge if it is rechargeable.

6.5.11 Monitoring ADC (MADC)

The MADC consists in a 10-bit analog to digital converter combined with a nine inputs analog multiplexer. Out of the nine inputs five are available externally, the four remaining being dedicated to main battery voltage, back up battery voltage, charger voltage and charger current monitoring. On the five available externally three are standard inputs intended for battery temperature, battery type measurements.

6.5.12 Reference Voltage / Power on Control (VRPC)

An integrated band-gap generates a reference voltage. This reference is available on an external pin for external filtering purpose only. This filtered reference is internally used for analog functions. The external resistor connected between pin IBIAS and GNDREF sets, from the band-gap voltage, the value of the bias currents of the analog functions. The VRPC block is in charge to control the Power ON, Power OFF, Switch On, and Switch OFF sequences. Even in Switch OFF state some blocks functions are performed. These “permanent” functions are functions, which insure the wake-up of the mobile such as ON/OFF button detection or charger detection. Interrupts are generated at power-down detection of the PWON button and when abnormal voltage conditions are detected.

6.5.13 Internal bus and interrupt controller (IBIC)

Read and write access to all internal registers being possible via both the BSP and USP, purpose of the internal bus controller is to arbitrate the access on the internal bus and to direct the read data to the proper serial port. During reception of a burst the internal bus controller assign the transmit part of the BSP to the base-band downlink to transfer the I & Q samples to the DSP.

7 Power Supply

Description:

The voltage regulators embedded in IOTA consists of seven sub blocks. Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital circuit, to DBB processor, and to external memory.

· LDO (VRDBB) is a programmable regulator that generates the supply voltages (1.8V,1.5V and 1.3V) for the core of the DBB processor. The main battery supplies VRDBB.

· LDO (VRIO) generate the supply voltage (2.8V) for the digital core and I/O of the TWL3025 device. The main battery supplies VRIO.

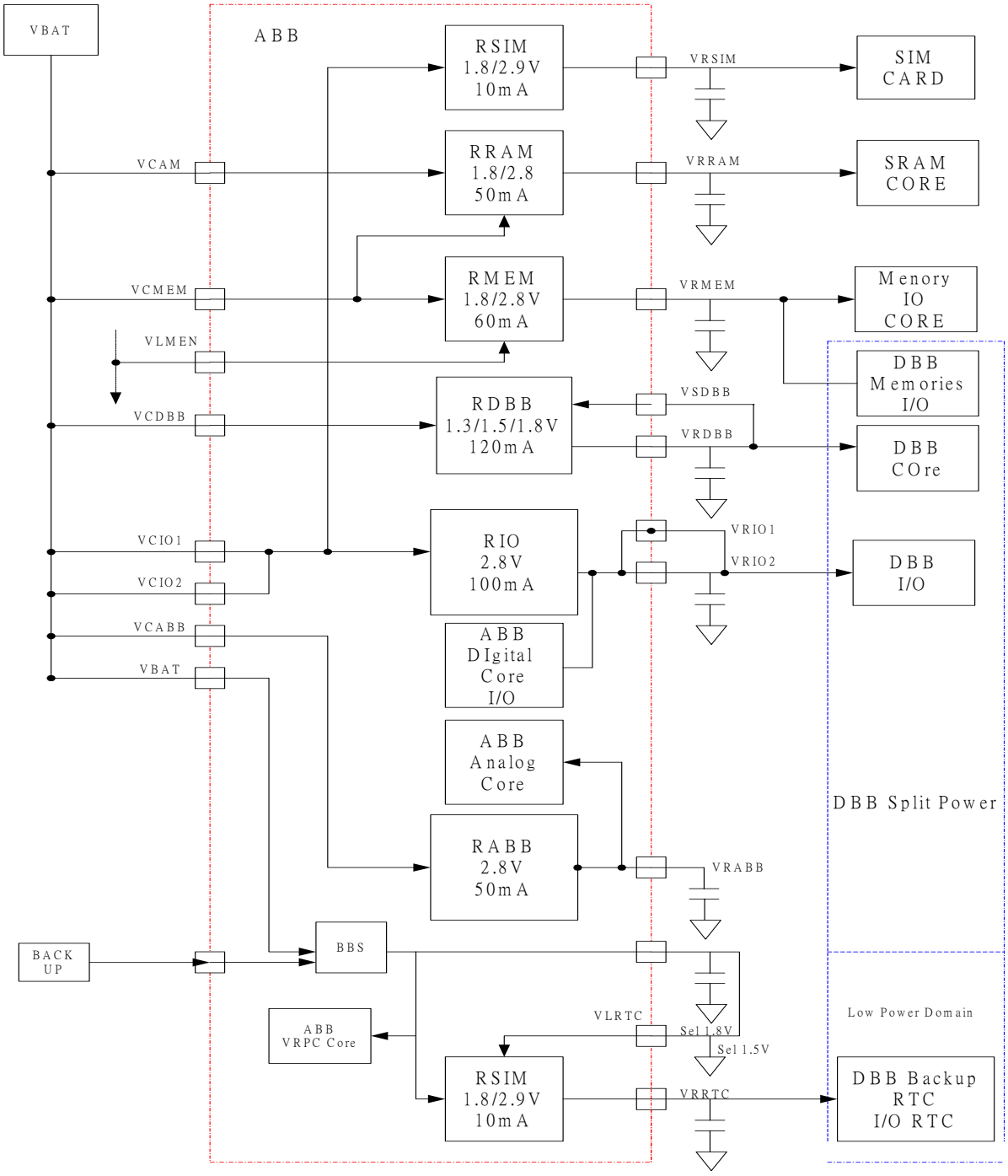
· LDO (VRMEM) is a programmable regulator that generates the supply voltages (2.8V and 1.8V) for external memories (typically flash memories) and DBB memory interface I/O. The main battery supplies VRMEM.

· LDO (VRRAM) is a programmable regulator that generate the supply voltages(2.8V and 1.8V) the external memory (typically SRAM memories) and DBB memory interface I/Os. The main battery supplies VRRAM.

· LDO (VRABB) generates the supply voltage (2.8V) for the analog functions of the TWL 3014 devices. The main battery supplies VRABB.

· LDO (VRSIM) is a programmable regulator that generates the supply voltages (2.9V and 1.8V) SIM card and SIM card devices. The main battery supplies VRSIM.

· LDO (VRTC) is a programmable regulator that generates the supply voltage (1.8V.1.5Vand 1.3V) for real time clock and the 32-KHZ oscillator located in the DBB device during all modes. The main or backup battery supplies VRTC.



System power on/off Sequence

Power on mode

On the plug-in of the valid main battery or backup battery, an internal reset is generated (POR). After a power-on sequence, the TWL3025 device is in the BACKUP or OFF state. When these conditions occur in the power on state, the hardware power on sequence starts:

1. Enable band-gap (VREF and IREF)
2. Check if Main Battery voltage is greater than 3.2V
3. Enable charge VRDBB-VRABB-VRMEM-VRRAM
4. Regulator OK.
5. ON_nOFF=1, ABB RSTz=1
6. NRESET pin is set from ‘L’ to ‘H’
7. 13MHz clock oscillator is enabled

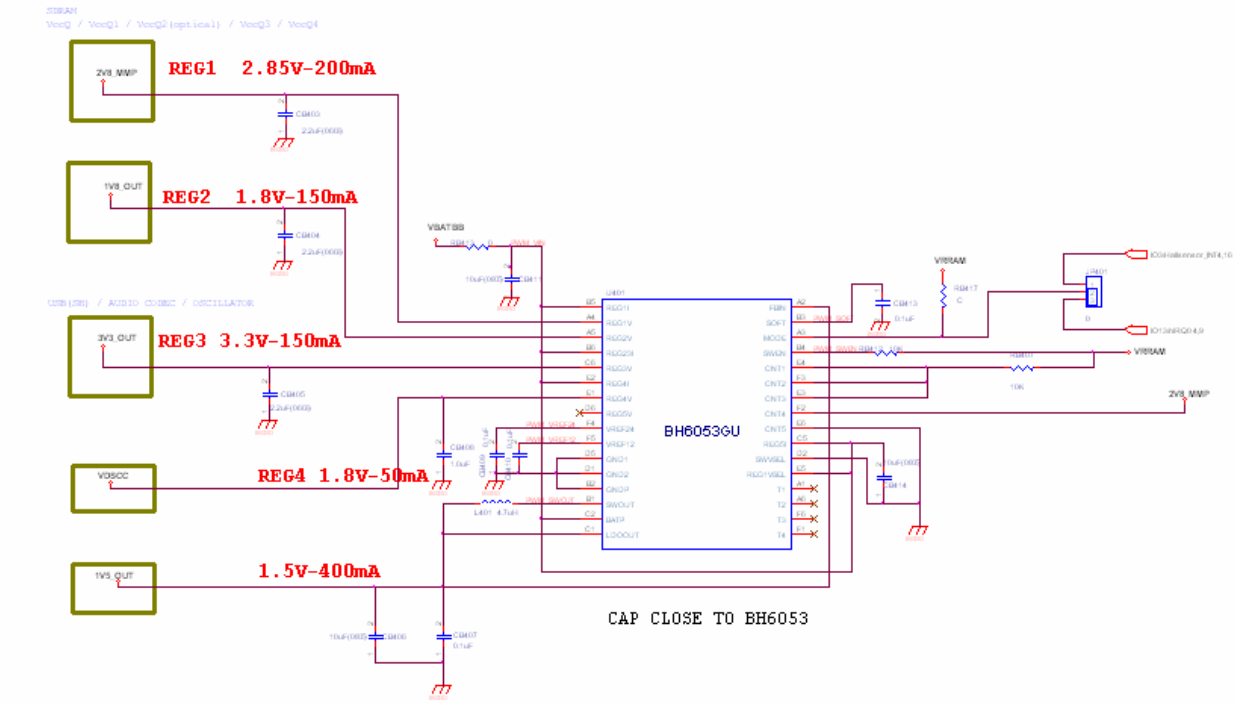
Power off mode

This state is reached when there is not enough voltage in the main battery and backup battery or when both batteries are disconnected.

1. Send INT1
2. Start 5*T watchdog Timer , T= 32K period
3. ON_nOFF=0
4. ABB RSTz=0
5. Disable the LDO’s using MSKOFF content and the band-gap
6. “MBATLOW”=0

MMP Power—Rohm PMIC

7.3.1 PMIC schematic



Description:

Rohm power management IC BH6053GU is designed for MMP.
BH6053GU provides voltages 2.8V , 1.8V, 1.5V and 3.3V for Multimedia processor (MMP), DSC module , LCD module, NAND FLASH and audio CODEC.

8 MMP

SH7327

This LSI is a single-chip RISC microprocessor that integrates an extended 32-bit RISC-type SuperH architecture CPU with a digital signal processing (DSP) extension as its core, together with a large-capacity 32-kbyte cache memory, a 16-kbyte X/Y memory, a 32-kbyte U memory, and an interrupt controller.
High-speed data transfers can be performed by an on-chip direct memory access controller (DMAC), and an external memory access support function enables direct connection to different kinds of memory. This LSI also includes powerful peripheral functions that are essential to system configuration, such as a serial interface which has a large FIFO.
Moreover, this LSI realizes various functions which are needed for the next generation of mobile phone applications, such as an easy-to-use camera interface, sound input/output, MPEG4 encoding/decoding accelerator, and USB function module. A powerful built-in power-management function keeps power consumption low, even during high-speed operation. This LSI is ideal for use in electronic devices such as those for applications that require both high-speed operation and low power consumption simultaneously.

9 Three combo memory

Description:

The M6MGA157F2LCWG consists of 128M-bit NOR type Flash memory, 256M-bit superAND Flash memory and 64Mbit mobileRAM in a 144-ball Stacked CSP(Chip Scale Package) for lead free use.
128M-bit NOR type Flash memory is a high performance non-volatile memory having the advantage of BGO function. 256M-bit superAND Flash memory is a high performance non-volatile memory, which uses AND type multi-level memory cell. The superAND Flash memory doesn't need complicated operations such as sector management for defect sector and error check correction.
64M-bit mobileRAM is a 4,194,304 words high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM. The M6MGA157F2LCWG is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.
The 128-Mbit NOR type Flash Memory 3rd Generation is a high-performance 134,217,728-bit CMOS boot block Flash memory device, organized as 8,388,608-word by 16-bit. The device uses a single VCC of 2.7 V to 3.0 V to perform read, erase and program operations. The device supports alternating Background Operation (BGO). By dividing the 128-Mbit memory space into six banks, the device is capable of reading data from one bank while programming, erasing, software command writing, or data loading in one of the other five banks. This feature allows a host system to perform code pre-fetching in one bank while background programming or erasing data in another bank.

It is suitable for communication products and cellular phones. The device also provides high-performance eight-word page reads. The device is manufactured using the architecture that enables fast erase operations (0.1 seconds per block).
256M superAND Flash Memory is a CMOS flash memory, which uses cost effective and high performance AND type multi-level memory cell technology. Current AND flash memory requires us to support complicated operations such as sector management for defect sector and error check correction. But this Flash Memory doesn't need such operations. Beside it supports wear leveling function, which is sector replacement function in case of that certain sector, reaches certain erase/write times. And auto read function is available. It enables to read the data without command and address input.
64M-bit mobileRAM is a 4,194,304-word high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM. The cells are automatically refreshed and the refresh control is not required for system. The device also has the partial block refresh scheme and the power down mode by writing the command. The RENESAS mobileRAM is suitable for a high performance cellular phone and a mobile PC requiring small mounting area, light weight and low power dissipation.

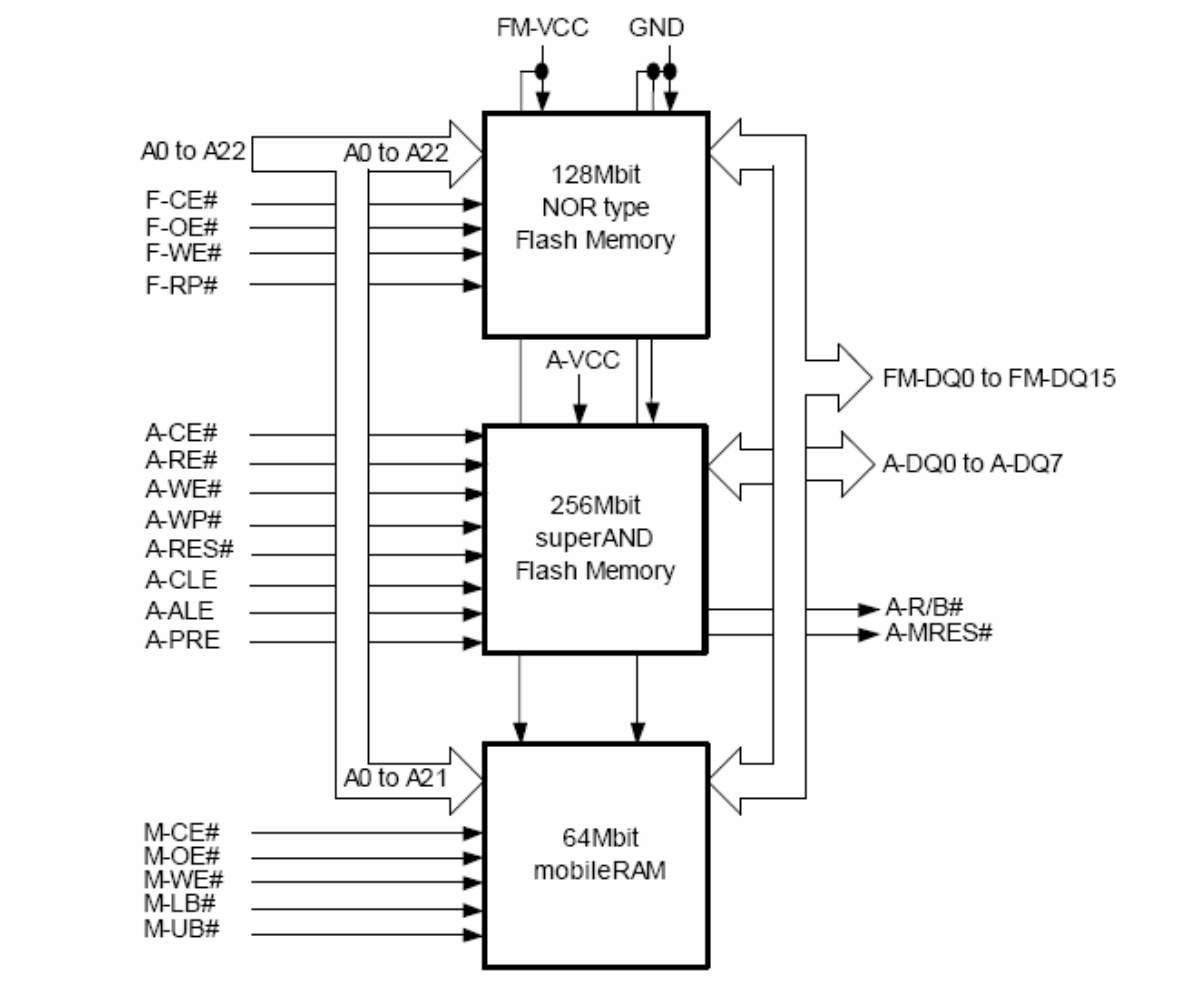
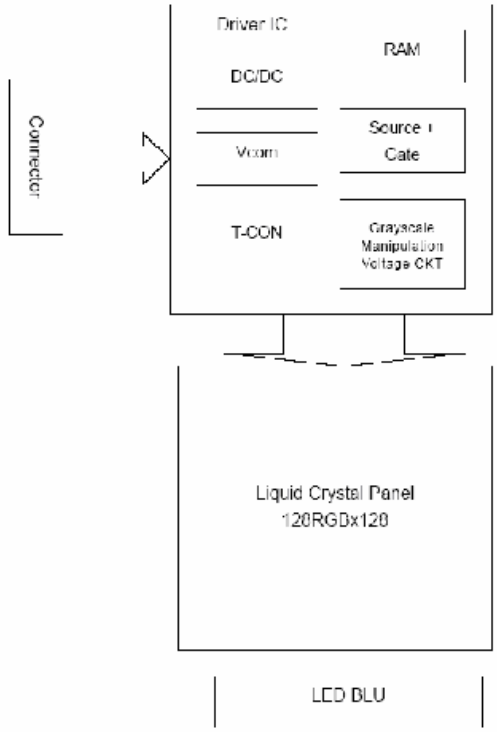


Figure 4. MCP BLOCK DIAGRAM

10 Display

Block diagram



Key features

a. Allows direct RAM data display (RAM is included in the source driver):
A single pixel consists of three dots (RGB), and a single dot consists of 6 bits data (64 gray-scale). Built-in RAM capacity are 132x3x132x6=313,632 bits
b. Can display moving pictures up to 30 FPS, and support area scrolling and partial display
c. Can support 8/9/16/18 bits parallel i80 series CPU interface
d. Reserve the flexibility for making dual-display module
e. Low power consumption and single chip driver solution

11 Audio Codec and Audio Amplifier

9.1 Audio Codec Function Block

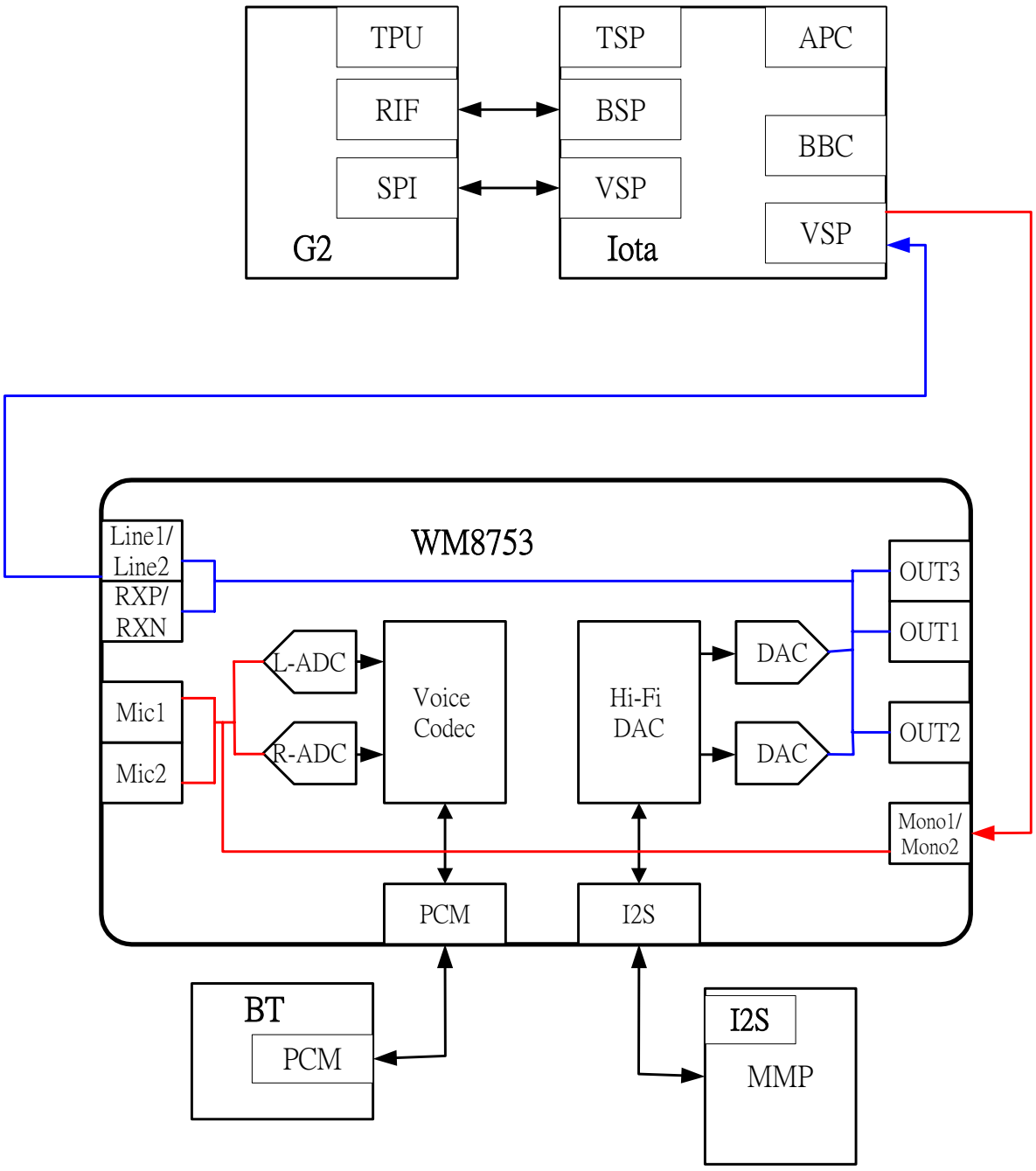
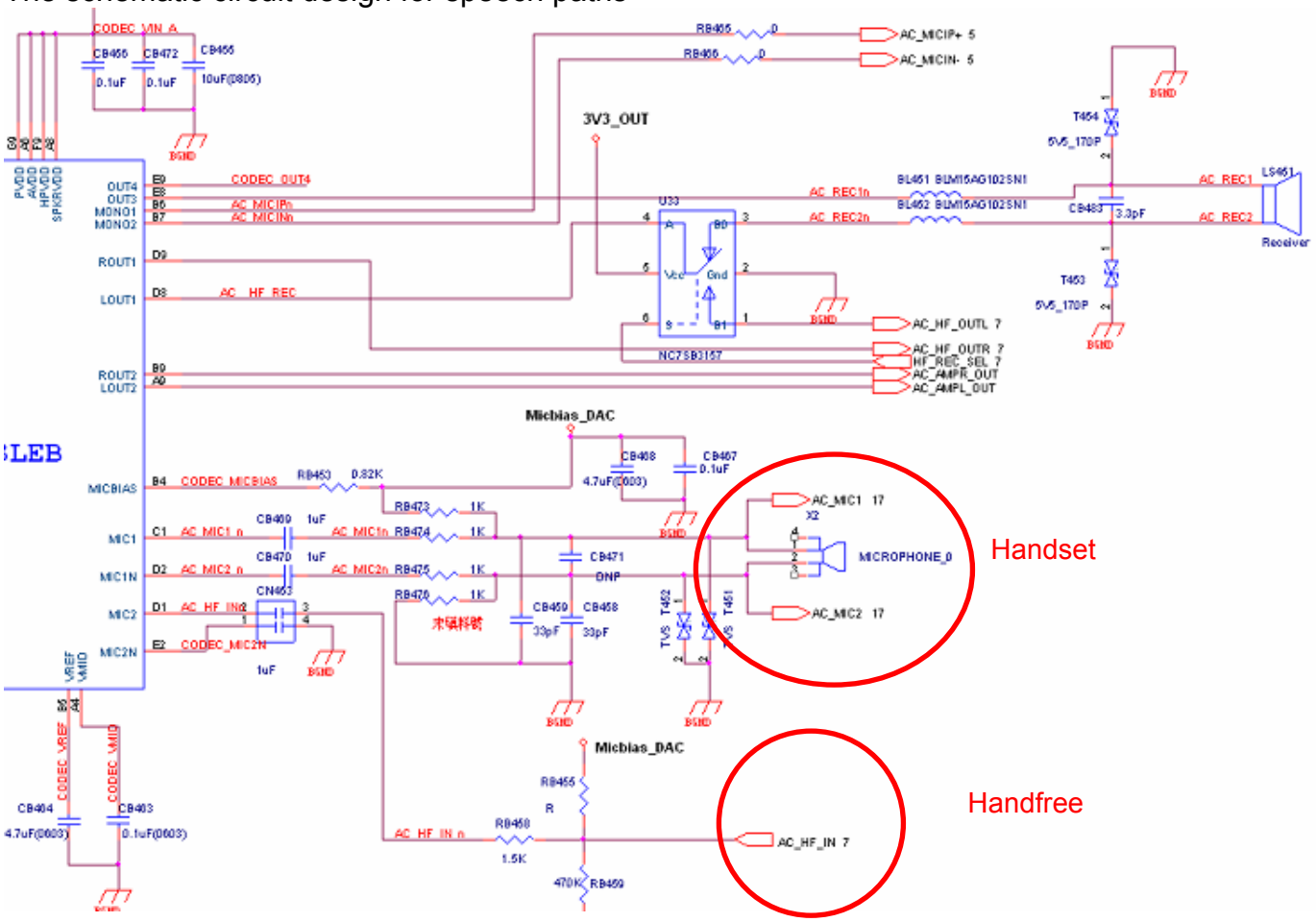


Fig 1 Audio codec design block diagram

The audio circuit uses the Wolfson WM8753 for audio total solution. The WM8753 is a low power, high quality stereo Codec with integrated voice CODEC designed for portable digital telephony application with Hi-Fi playback capability. The device integrates dual interfaces to two differentially connected microphones, and includes drivers for speakers, headphone and earpiece. Advanced on-chip digital signal processing performs tone control, Bass Boost and automatic level control for the microphone or line output through the ADC. The two ADCs may be used to support Voice noise cancellation in a partnering DSP, or for stereo recording.

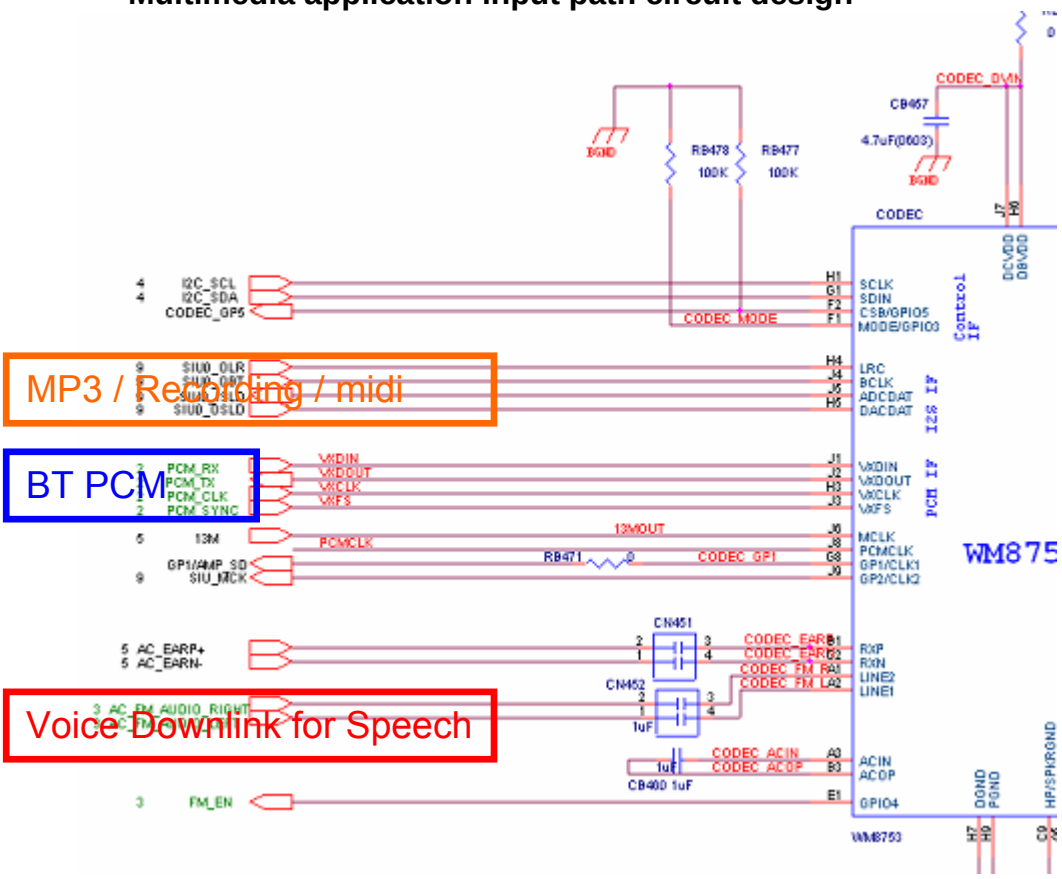
So that all the voice signals, digital and analog, sink in the coedec WM8753. For MP3 ,software midi playback ,and audio recording, the I2S interface provides a connection with the MMP. And it connects to analog base-band voice codec for mobile phone speech process. It uses the PCM interface to support the BlueTooth voice solution.

The schematic circuit design for speech paths



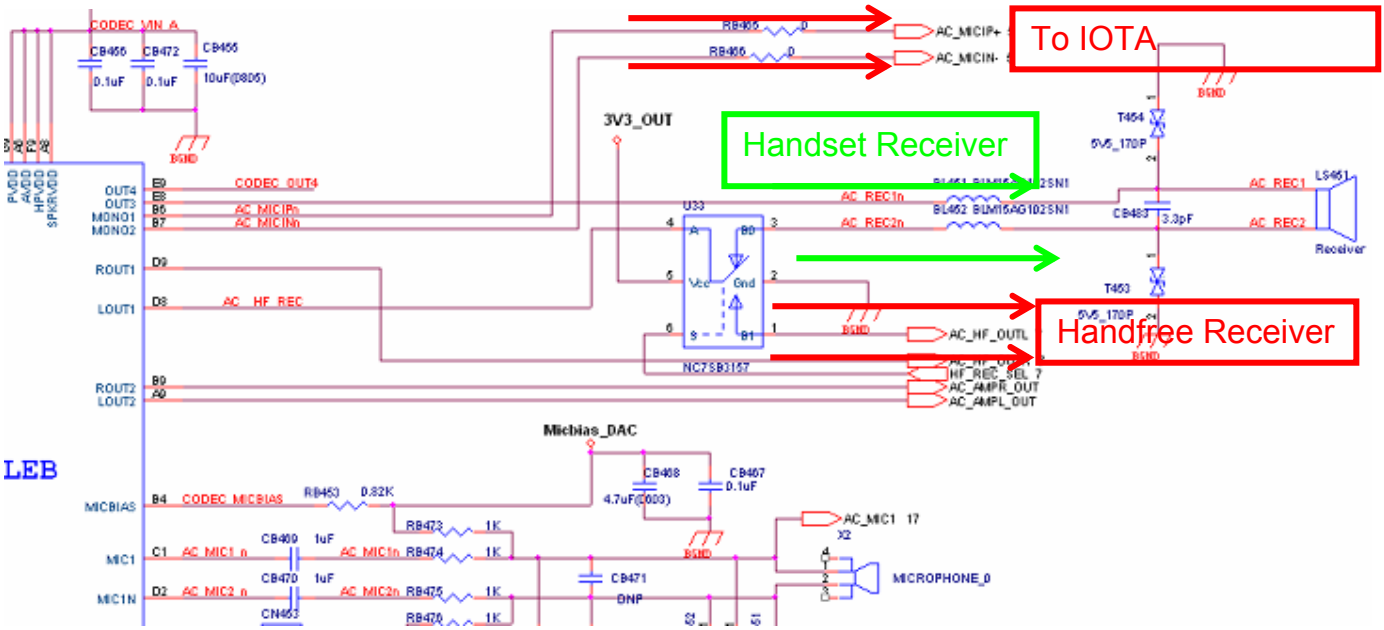
The voice input used to audio codec microphone port transmission the voice signal. Microphone input path to handheld and handfree application (Fig 2). The handheld used to differential input for main path .However handfree used to signal input transmission voice the uplink path.

Multimedia application input path circuit design

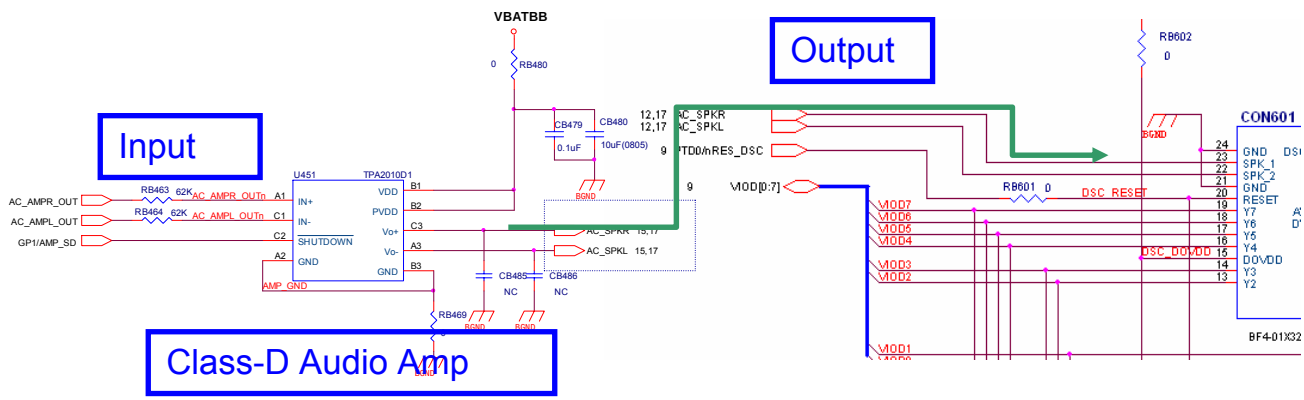


The Fig 3 provides audio codec input path circuit design , The two signal input used to voice path apply to bypass IOTA downlink signal and FM radio. However one differential input path used to melody function the transmission. The MP3 and Recoder to utilize audio codec digital input control, data transmission the I2C digital voice input transfer ,the I2C control for audio codec command .

Multimedia application output path circuit design



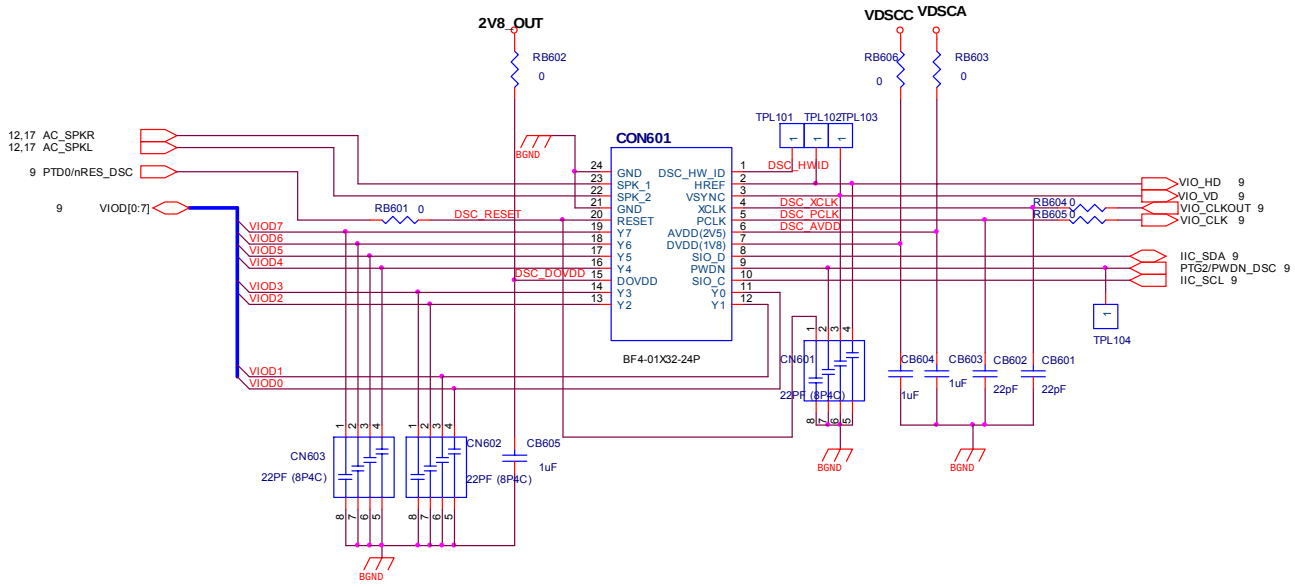
Loudspeaker output path and D-amplifier design



The audio codec provides output path application (Fig 4), two mono output and one stereo output. A mono output use so d to differential signal apply to uplink voice output transfer IOTA produce . The mono2 output used to differential signal for Loukspeaker function ,but design addition the D amplifier (Fig 5) for gain amplifier provides MP3 play ,melody and speaker phone function the application .
The stereo output apply to handfree part. However downlink output path used to control WM8753 the OUT3 path transfer receiver function for the user receive downlink voice. So the another output provides downlink path used to handfree function by user application design .
The Class-D audio amplifier has a high efficiency of the power transformation. It drivers a 18mm diameter loudspeaker for MP3 playback or hand free speech mode. It also supports saving the power dissipation by the codec WM8753.

12 Camera

DSC Connector and Pin Assignment



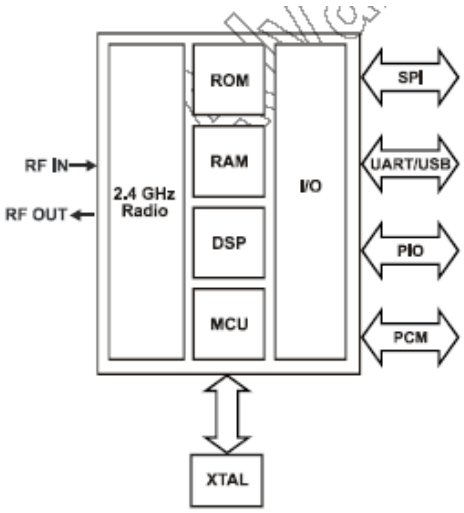
Description

The camera module (CM-5627) is sensor on-board camera and lens module designed for mobile application where low power consumption and small size are of utmost importance. Proprietary OV7660 sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions are programmable through the Serial Camera Control Bus (SCCB) interface. The device can be programmed to provide image output in various fully processed and encoded formats.

2.pin assignment

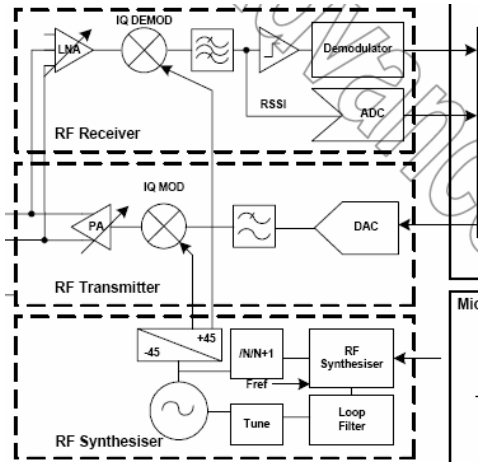
Pin Number	Name	Pin Type	Function Description
1	DSC_HW_ID	F	Module vendor detect
2	HREF	Output	HREF output
3	VSYNC	O	Vertical sync output
4	XCLK	I	Clock input
5	PCLK	O	Pixel clock output
6	AVDD	P	Analog Power (2.5V)
7	DVDD	P	Power supply (1.8VDC for digital logic core)
8	SIO_D	I/O	SCCB serial interface data input and output
9	PWDN	F	Power Down Mode Selection 0: Normal mode 1: Power down mode
10	SIO_C	I	SCCB serial interface clock input
11	Y0	O	Output Video component output bit[0]
12	Y1	O	Output Video component output bit[1]
13	GND	P	Ground
14	SPK_1	SPK+	P+
15	SPK_2	SPK-	P-
16	GND	P	Ground
17	RESET	F	Chip reset, with active high
18	Y7	O	Output Video component output bit[7]
19	Y6	O	Output Video component output bit[6]
20	Y5	O	Output Video component output bit[5]
21	Y4	O	Output Video component output bit[4]
22	DOVDD	P	Digital I/O power (2.25V to 3.6V)
23	Y3	O	Output Video component output bit[3]
24	Y2	O	Output Video component output bit[2]

13 Bluetooth



BlueCore3-ROM CSP is a single chip radio andbase band chip for Bluetooth wireless technology2.4GHz systems. It is implemented in 0.18µm
CMOS technology.BlueCore3-ROM CSP has been designed to reduce the
Number of external components required, which ensures Production costs are minimized.
The device incorporates auto-calibration and built-in Self-test (BIST) routines to simplify development, type Approval and production test. All hardware and device firmware is fully compliant with the Blue tooth specification v1.2.

Description of Functional Blocks
RF Receiver
The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitized. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-ROM CSP to exceed the Blue tooth requirements for Co-channel and adjacent channel rejection.



Low Noise Amplifier
The LNA operates in differential mode and is used for Class 2 operation.
Analogue to Digital Converter
The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain ischanged according to the measured RSSI value, keeping the first mixer input signal within a limited range. ThisImproves the dynamic range of the receiver, improving performance in interference limited environments.

RF Transmitter

IQ Modulator

The transmitter features a direct IQ modulator to minimize the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital base band transmit filter provides the required spectral shaping.

Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-ROM CSP to be used in Class 2 and Class 3 radios without an external RF PA.

RF Synthesizer

The radio synthesizer is fully integrated onto the die with no requirement for an external Voltage Controlled
Oscillator (VCO) screening can, varactor tuning diodes or LC resonators. The synthesizer is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Blue tooth specification V1.2.

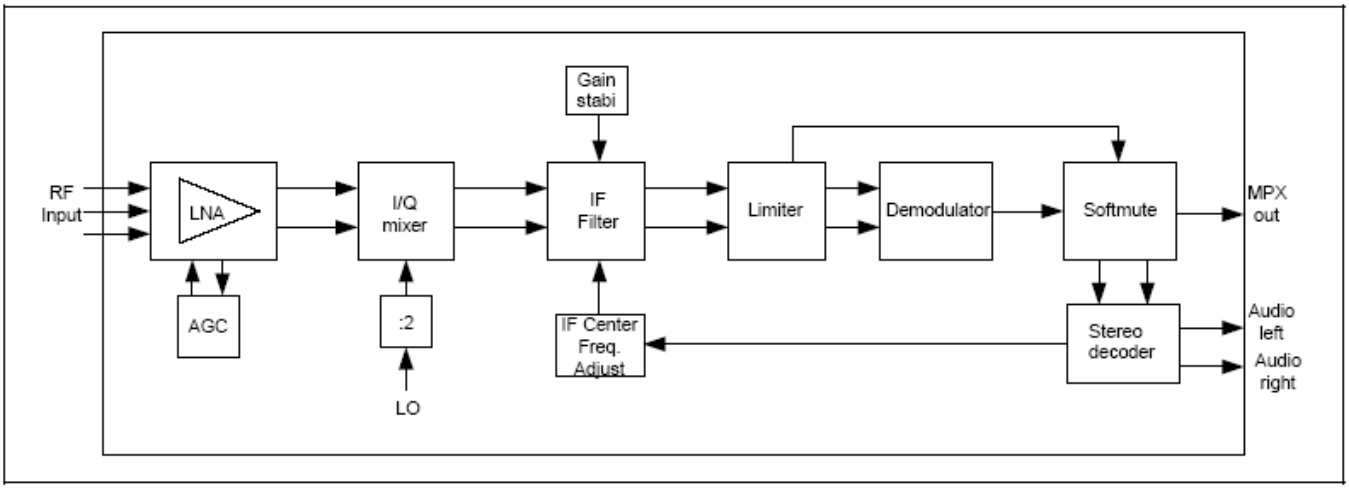
Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

14 FM Radio

TEA5767HN

The TEA5767HN consists of three major blocks: the signal channel, the tuning system and the bus interface. In
this chapter the signal channel will be described briefly.



Low Noise Amplifier

The TEA5767HN has an integrated low noise amplifier (LNA). This is a balanced amplifier, which is less sensible for common mode noise. The input impedance of the LNA is (100Ω||4pF) each pin (referenced to ground).To handle high level input signals, the gain of the LNA is controlled by means of an automatic gain controller (AGC). The AGC will be

started when the antenna input reaches a level of about 4mV with a given application of 40Ω antenna impedance. The AGC has a range of 40dB.

Mixer
The TEA5767HN has a complex mixer. This mixer receives two RF signals directly from the LNA and delivers two signals with an intermediate frequency of 225 KHz. The mixer output signals comprise an in-phase component (00) and a quadrate component (90o).

IF selectivity
The selectivity is provided by a band pass filter with a low intermediate frequency (IF). This IF filter is fully integrated, which results in an alignment-free selectivity. The center frequency of this filter is 225 KHz and has a –3dB bandwidth of 90KHz.At 200 KHz from the center frequency, the IF filter selectivity is about 40dB.
The center frequency of the IF filter is internally adjusted in order to remove the influence of process spread.

Limiter
The limiter is DC coupled with feedback capacitors on pin 28 and 29. These capacitors build a low pass filter.

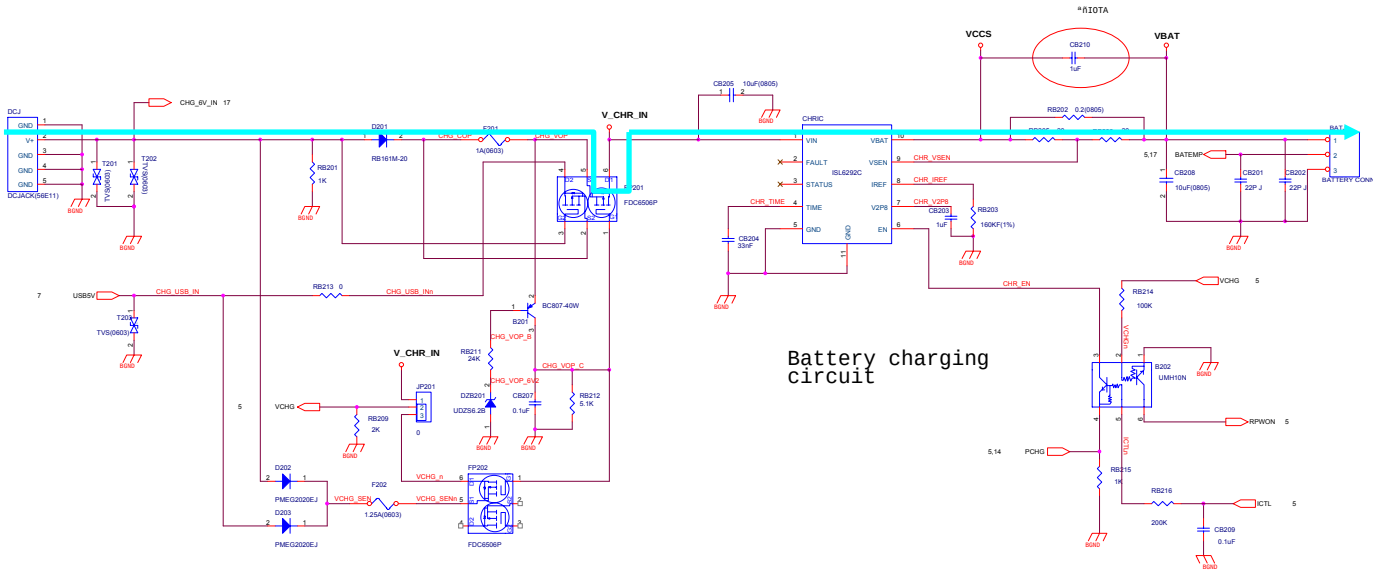
Demodulator
The demodulator is also fully integrated. The advantage of this is that no alignment will be necessary.
The demodulator has a conversion factor of 75mV at 22.5kHz.

15 Battery

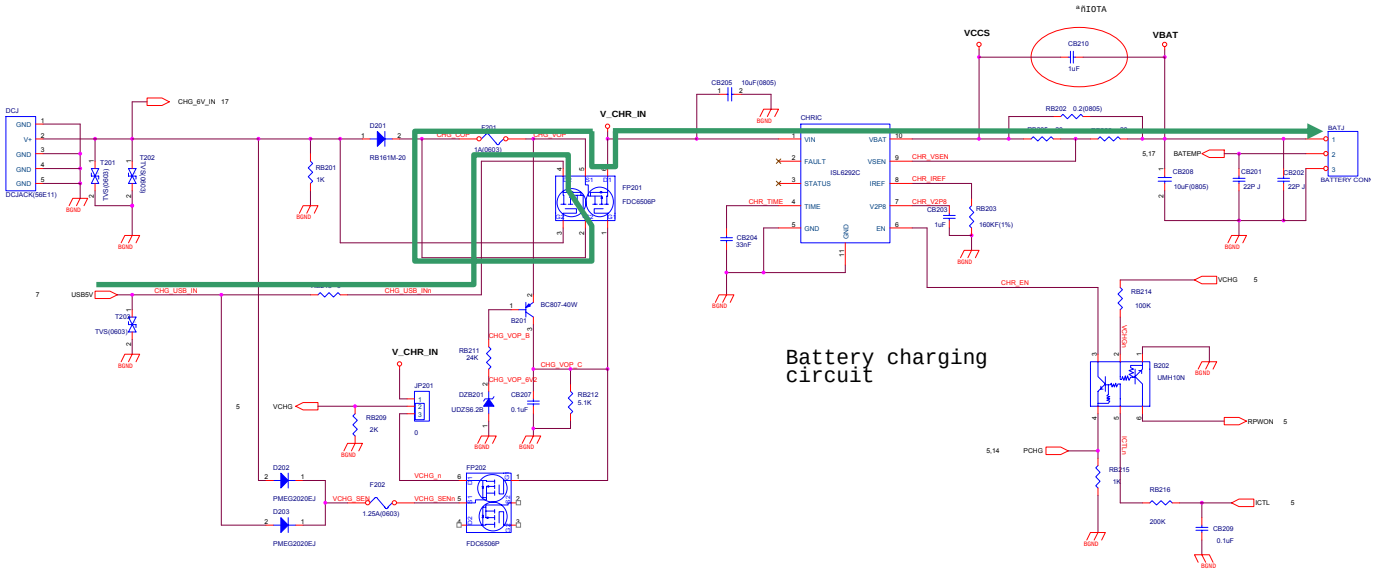
Description	Specification	Unit	Condition
Nominal Capacity	920	mAh	Discharged at 0.2C to 2.75V after standard charge at 25℃
Nominal Voltage	3.7	V	
Discharge End Voltage	2.75V / cell	V	
Maximum charging temp.	45	°C	
Minimum charging temp.	0	°C	
Charging voltage protection	6.9+/-0.1	V	
Battery voltage protection	4.325+/-0.025	V	
Charging Current (Std.)	500	mA	0~45°C
Charging Current (Max.)	920	mA	0~45°C
Charging complete Voltage	4.2±0.05	V	
Maximum Charging Time	5	Hour	
Discharge Current (Max.)	1380	mA	-20~+60°C
Total Internal Resistance	<70	mΩ	AC 1k Hz
Storage Temperature and humidity range	-20~+50 , 65+-20%	°C , RH	Less than 30 days
	-20~+35 , 65+-20%	°C , RH	Less than 90 days

15.1 Charging Concept

Schematic



Charging from AC Adaptor



Charging from USB

Description

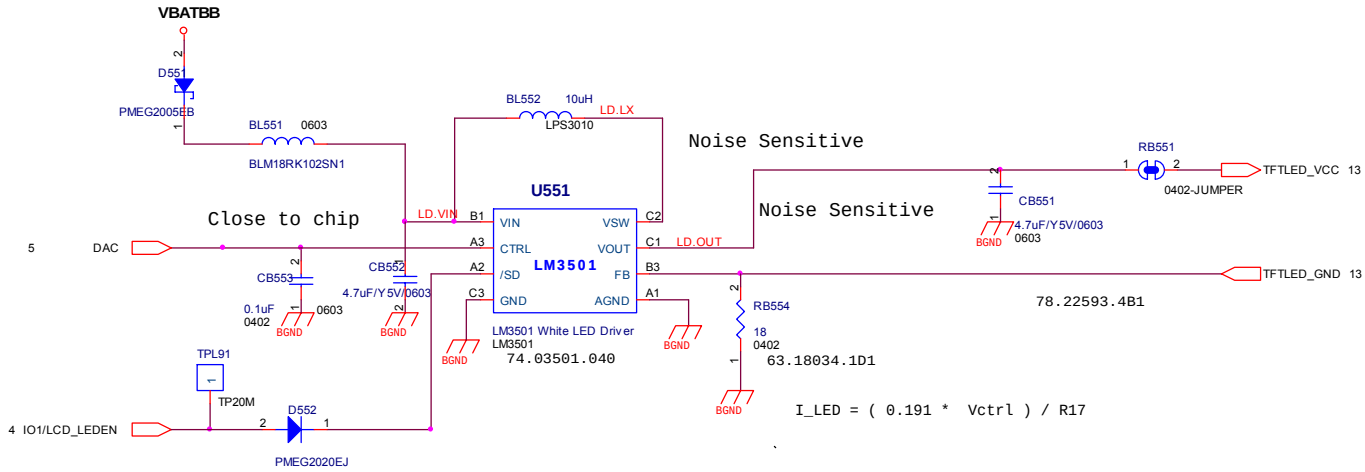
PANB2A can charge the Li-ion/Li Polymer Battery from AC adaptor and USB, As Fig 3.10.1, blue line is the charging route from adaptor show the route of USB and Fig 3.10.2, green line is the charging route from USB. While USB and adaptor have plugged in at the same time, FP201 allows charging only from adaptor. D201 avoids charging current flowing back to adaptor when USB is charging. Over voltage protection can be done by DZB201, B201 and FP201 whatever adaptor or USB is plugged in, there will be a voltage on VCHG pin, VCHG informs IOTA adaptor or USB is plugged in and IOTA controls CHRIC by ICTL and PCHG .CHRIC, Intersil ISL 6292C is described as below.

Li-ion/Li Polymer Battery Charger ISL6262C

The ISL6292C is an integrated single-cell Li-ion or Li polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of ac adapters or a USB port.
The ISL6292C operates as a linear charger when the ac adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 1.5A. The ISL6292C can also work with a current-limited adapter to minimize the thermal dissipation, in which case the ISL6292C combines the benefits of both a linear charger and a pulse charger. The ISL6292C features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery, automatic recharge, and thermally enhanced DFN package.

16 Illumination

Schematic

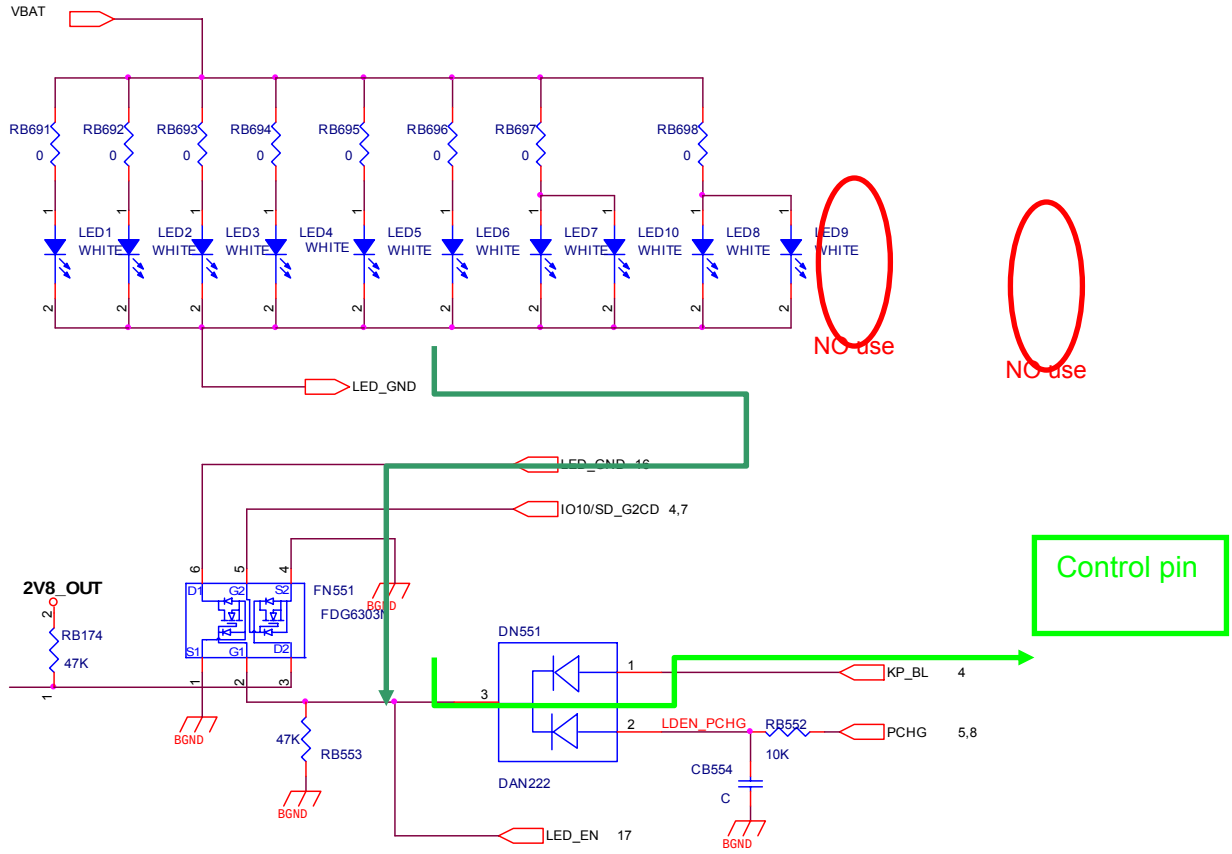


Description

The LM3501 is a fixed frequency synchronous step-up DC/DC converter in a small 8-bump thin micro SMD package. The LM3501 is ideal for white LED applications for cellular phone back-lighting requiring low current and high efficiency. Its fixed 1MHz operating frequency allows the use of small, low ESR capacitors as well as a more predictable frequency spectrum, which is important in cellular phone applications. The LM3501 can drive 2 to 4 white LEDs in series from a single Li-Ion battery or 3 cell NiMH with no external rectification diode. For white LED applications, a single external resistor is used to set the maximum LED current. The white LED current can easily be adjusted using an external voltage signal from a DAC or micro-controller. The LM3501 uses special protection circuitry on the output to prevent an overvoltage event if the primary white LED network should be disconnected eliminating the need of an extra protection Zener diode. In shutdown, the LM3501 disconnects the input and output creating a true isolation preventing any LED light from emitting over the full input operating voltage range and temperature.

17 Keypad LED circuit

Schematic

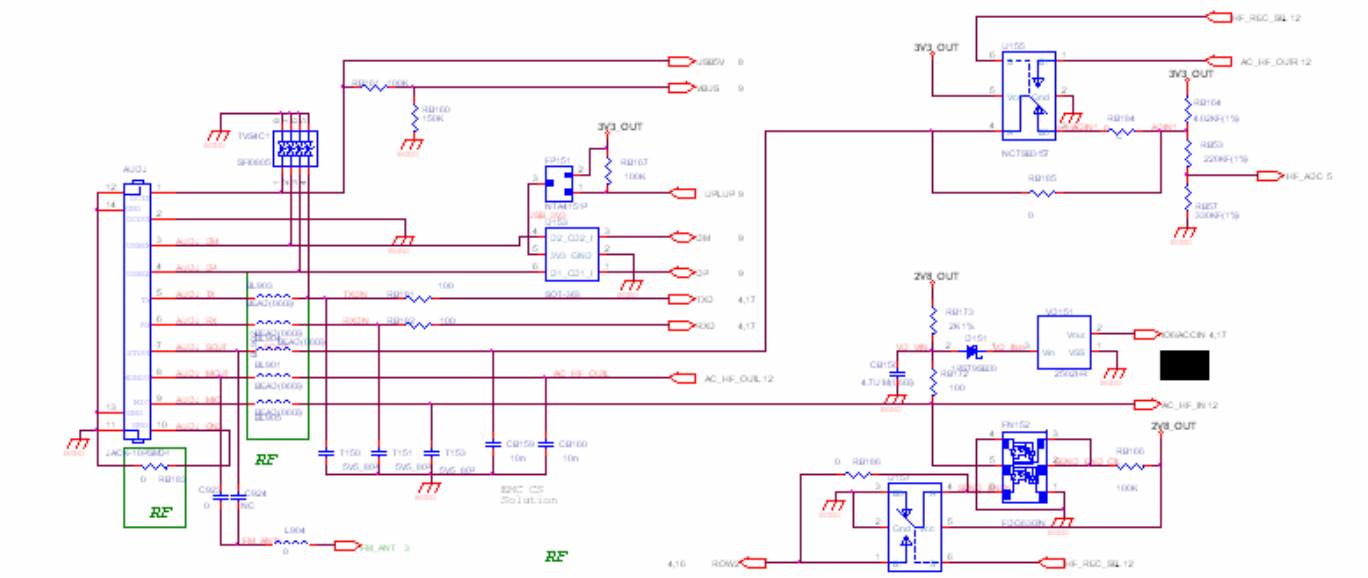


Description

PANB2A employs ten white LEDs for keypad backlight. The ON_OFF timing of LED is controlled by FN551. When KP_BL are set to “H”, Keypad LEDs are turned on; otherwise the Keypad LEDs are turned off.

18 Interfaces

Schematic



Pin No.	Pin Definition	Function description
1	DC in/USB 5V	External accessory power supply to the mobile phone
2	DC out(default)	Internal power provides for any powered accessory
3	USB data -	USB differential data line: D-
4	USB data +	USB differential data line: D+
5	UART Tx	UART data out line
6	UART Rx	UART data in line
7	Stereo out(right channel)	Use of the right audio path of the handfree and the accessory plug in detection
8	Mono out(left channel)	The left audio path of the handfree
9	Mic	The microphone of the handfree
10	Ground	Connect to system ground

3.8 .2 Description

The 10pin I/O Jack is used for 4 kinds of BenQ type accessory service: mono headset, stereo headset, UART data cable, and pure USB cable. Whenever the accessory plugs into the mobile, the IO6 will be pull to low level. And then according to the difference identified resistances mounted on the accessory, the system will get the difference ADC value from the EARPHONE_IN pin and recognize what type accessory has plugged in. In non-plugged-in situation, the pin 9 always has 2.8v potential voltage, and the output pin is high level (2.8v). Until the accessory plugs in, the Vout connecting to IO6 will fall down to low level(0.0v). At the same time the line voltage is changed by the plugged in accessory. When the system polls low level from IO6, it will read the current line voltage and convert it to

digital value from the EARPHONE_IN pin. Each ADC value represent different type accessory.

Accessory_IN/IO6	2.8v	0.0v	0.0v	0.0v	0.0v
ID resistance	-	10k Ohm	6.34k Ohm	3.57k Ohm	1.4k Ohm
EARPHONE_IN	2.8v	1.9~2.1v	1.6~1.8v	1.25~1.45v	0.6~0.8v
STATUS	NO ACCESSORY	Pure USB Cable	Data Cable	Stereo HF	Mono HF

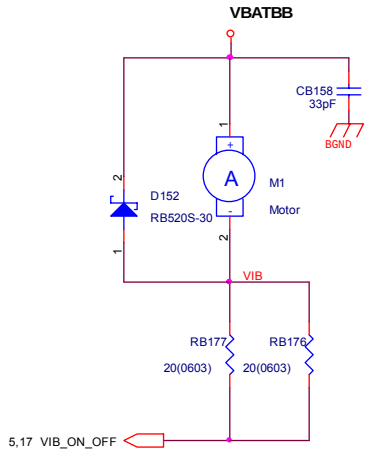
As we have seen, 10pin IO connector can provide each adaptive connectivity. Pure USB cable contribute to connect a master USB device; UART data cable provides to connect to a PC; also a mono or stereo type hand free can use to conversation whenever your hands are busy.

Pin No.	Pure USB	Data cable	Stereo HF	Mono HF
1	ˇ	ˇ		
2				
3	ˇ			
4	ˇ			
5		ˇ		
6		ˇ		
7	ˇ(10kΩ)	ˇ(6.34kΩ)	ˇ(3.57kΩ)	ˇ(1.4kΩ)
8			ˇ	ˇ
9	ˇ(2.2kΩ)	ˇ(2.2kΩ)	ˇ(Mic_R_dc)	ˇ(Mic_R_dc)
10	ˇ	ˇ	ˇ	ˇ

For audio type accessories, the microphone bias provides a mechanism to act on the send/end key for mono or stereo type accessory. When each kind of audio type accessory plugs in,U157 will connect to ROW2. Usually, ROW2 is high, Push the send/end key, it become to low.

19 Vibration Motor

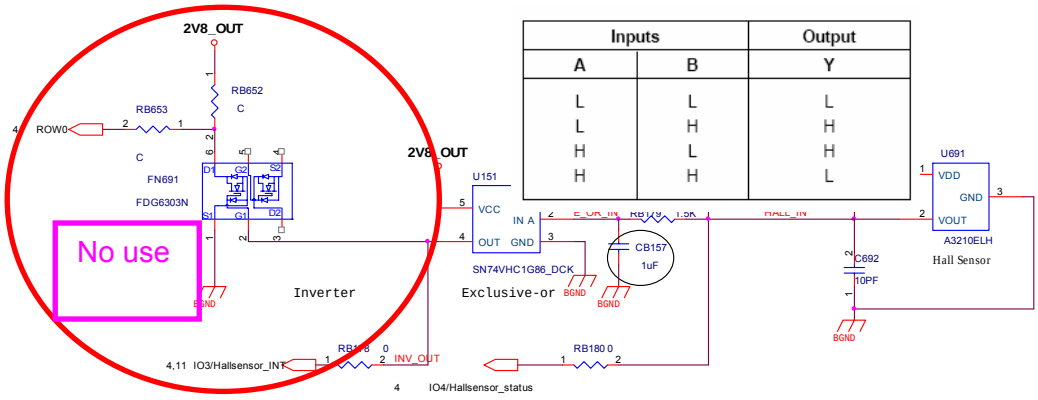
Schematic



Description
Vibrator is enabled by LEDB1 (LEDB2) control logic in IOTA. When the logic of LEDB is set to “H”, the vibrator will activate. The D4 is used to reduce EMF. The default VBAT is 3.8 volt.

20 Hall sensor

Schematic

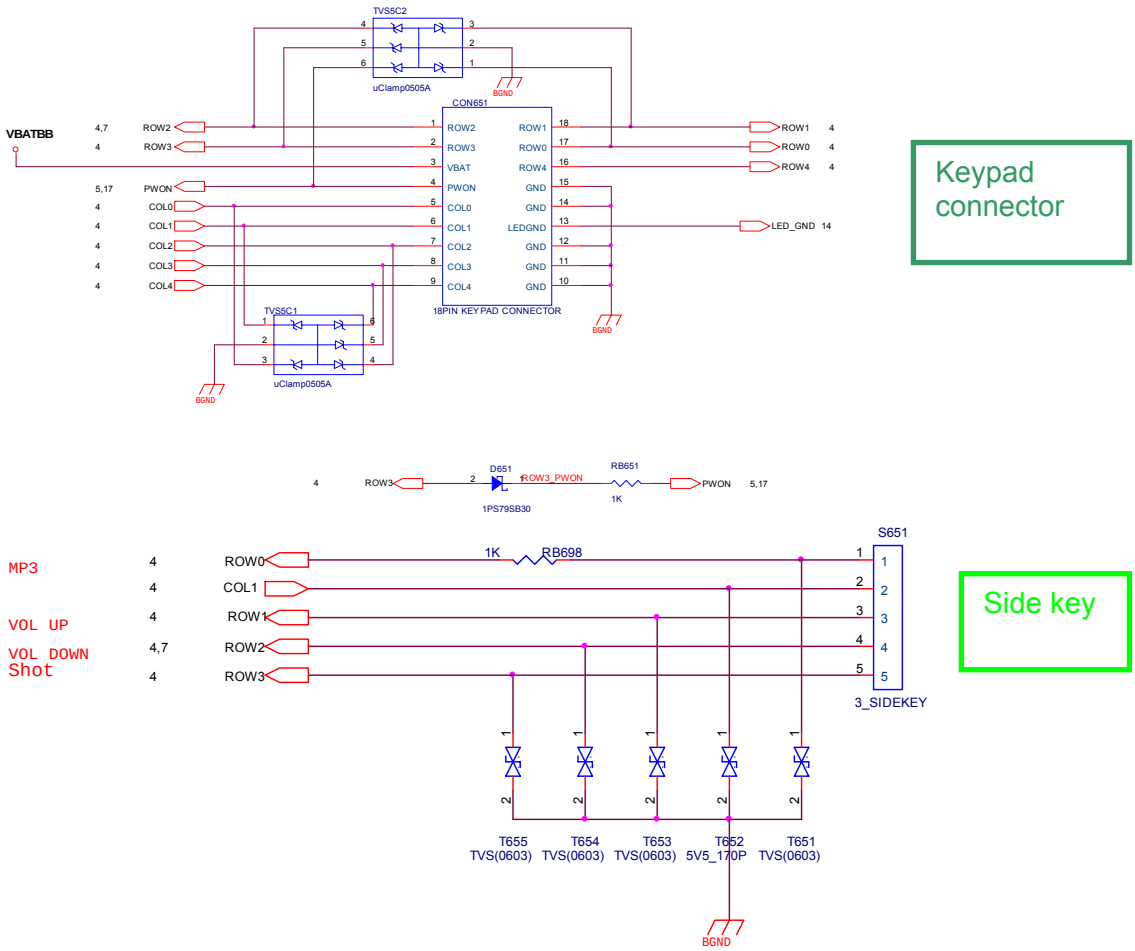


Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

3.18.2 Description
When flip change status change , IO3 will sent a interrupt signal to G2,then G2 will detect hall sensor status depend on IO4. If IO4 is High, flip close; otherwise flip close.

21 Keypad

Schematic



3.16.2 Description

The keypad is made of a 5 Column × 5 Row matrixes. The keypad matrix is as follows.

	COL0	COL1	COL2	COL3	COL4	
ROW0		VOL UP	3	2	1	
ROW1	SEND	VOL DOWN	6	5	4	
ROW2	SOFT LEFT	Shot	9	8	7	HF_S/E KEY
ROW3	SOFT RIGHT	MP3	#	0	*	END/POWER
ROW4	MENU	UP	LEFT	DOWN	RIGHT	

22 SD/MMC Minicard Reader

Mini SD card

3.9.1 Description:

T-Flash is a kind of SD-card (more little package)

3.9.1.1 SD Card Bus Topology

The SD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode. Host System can choose either one of modes. Same Data of the SD Card can read and write by both modes. SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss of performance, relatively to the SD mode.

3.9.1.2 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.

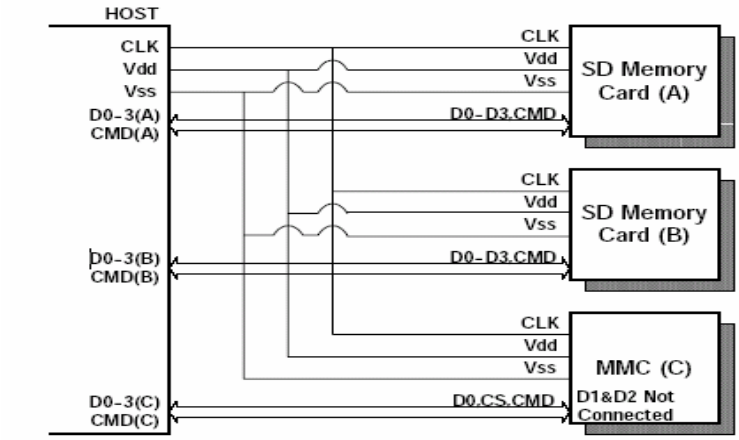
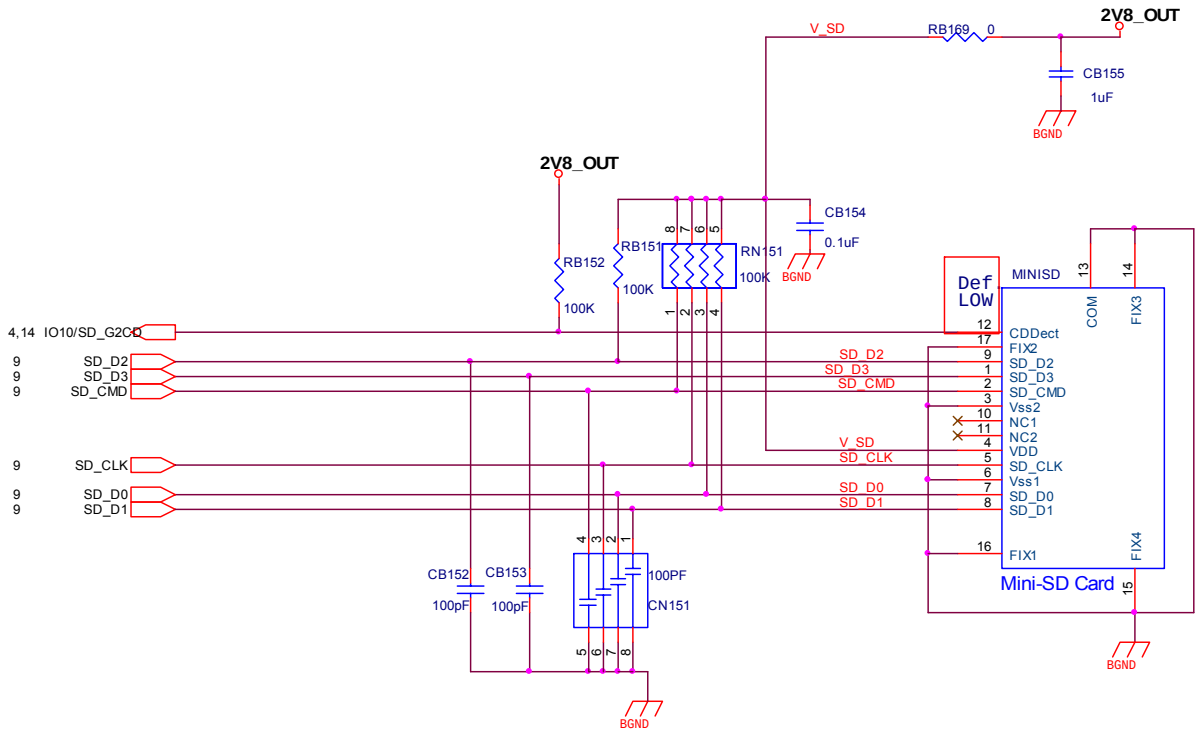


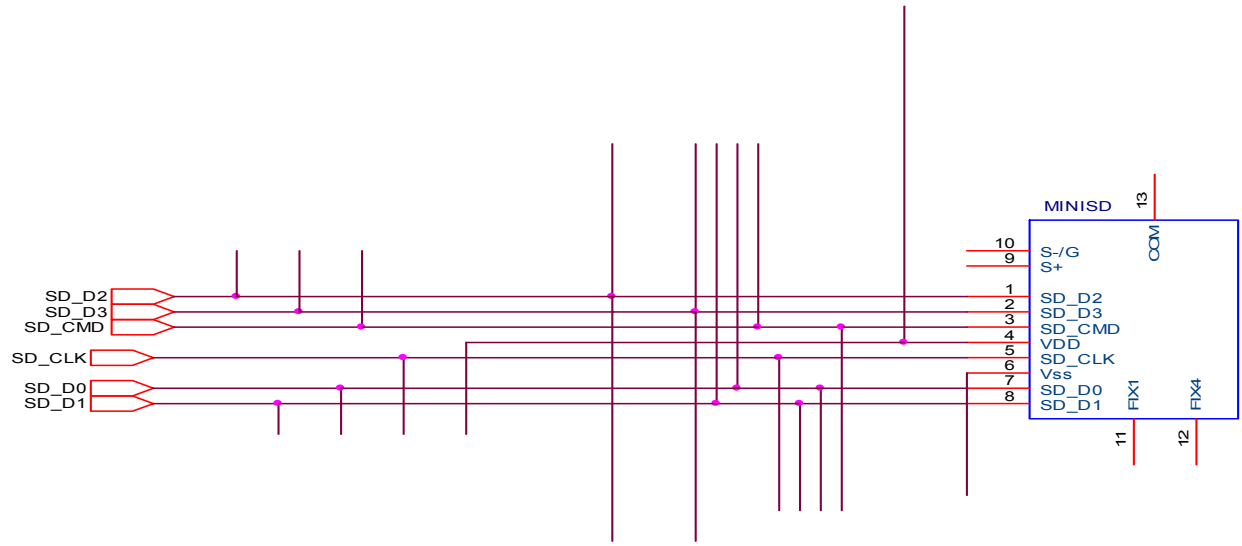
Fig 1: SD Card (SD Mode) connection Diagram

CLK: Host card Clock signal
CMD: Bi-directional Command/ Response Signal
DAT0 - DAT3: 4 Bi-directional data signal
Vdd: Power supply
Vs: GND

Schematic



SD Card Circuit



SD Card interface with SH Mobile (MMP)

Multiplied SD cards connections are available to the host. Common Vdd, Vss and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host. This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card.
Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from a addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

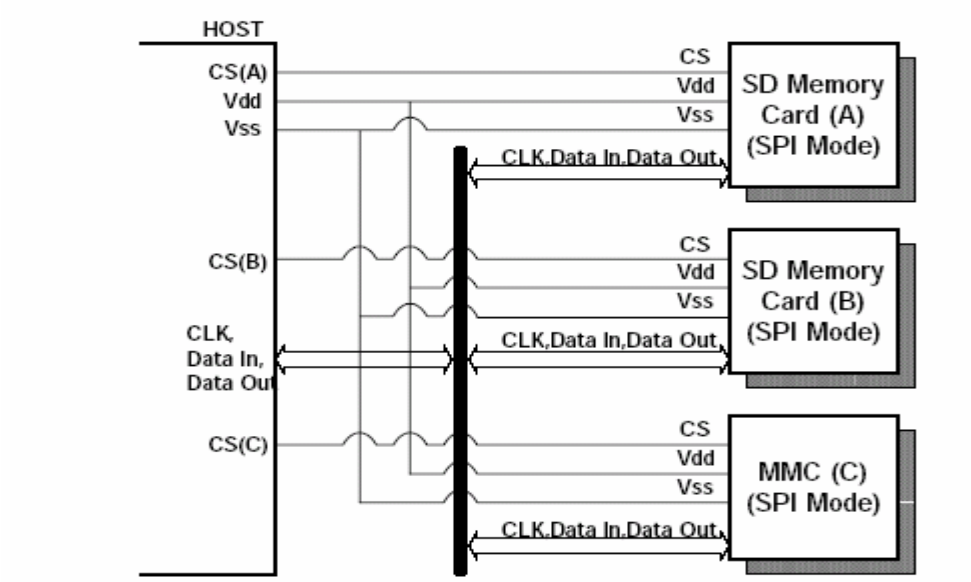


Fig 4: SD card (SPI mode) connection diagram

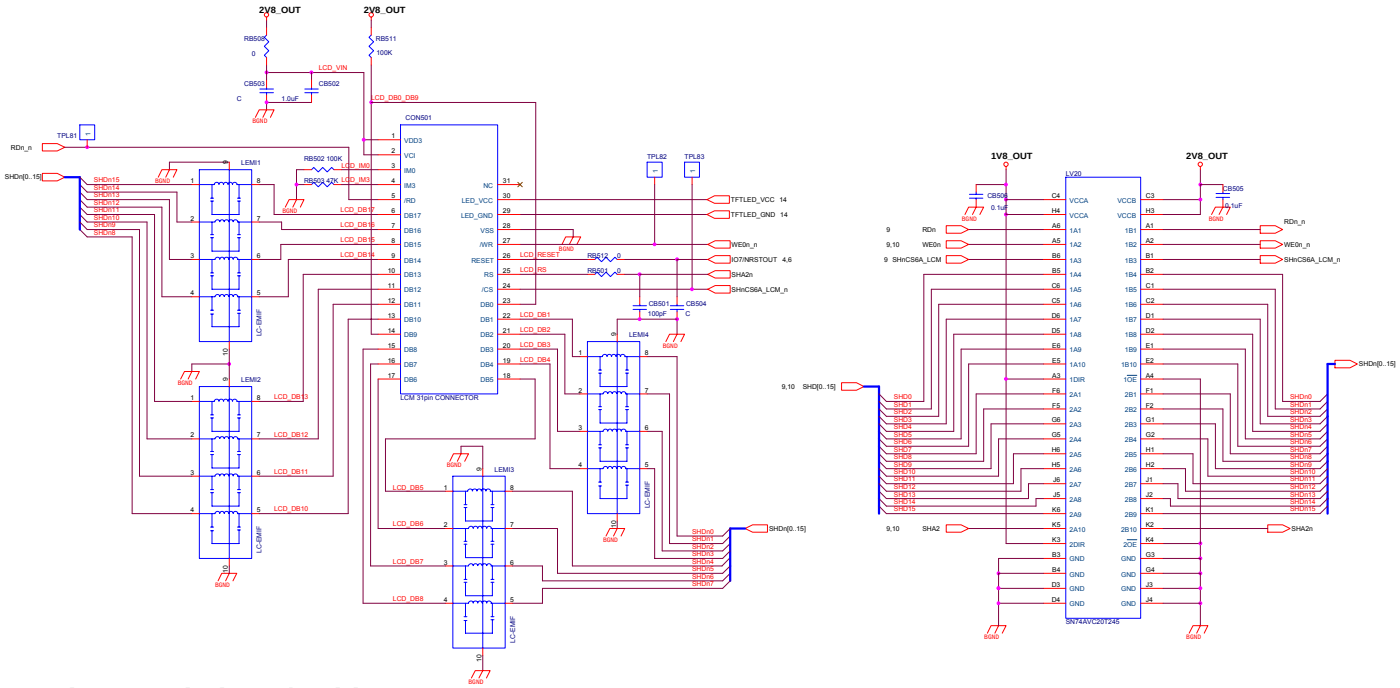
CS: Card Select Signal
CLK: Host card Clock signal
Data in: Host to card data line
Data out: card to host data line
Vdd: Power supply
Vss: GND

23 Camera Interface

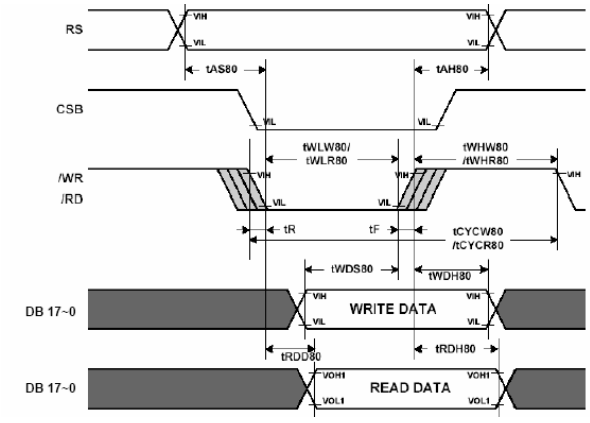
23.1 Display Connector

No	Pin name	I/O	Description	Remark
1	VDD3	-	2.3~3.3V(logic voltage range-regulated)	
2	VCI	I	2.5~3.3V(internal reference for power-supply)	
3	IM0	I	Pins to select interfacing mode with MPU When IM3="L"; IM0="L" is i80-system 16 bits (DB17-10,DB8-1) When IM3="L"; IM0="H" is i80-system 8 bits (DB17-10)	
4	IM3	I	Pins to select interfacing mode with MPU When IM3= "H"; IM0="L" is i80-system 18 bits (DB17-0) When IM3= "H"; IM0="H" is i80-system 9 bits (DB17-9)	
5	/RD	I	i80-system Read strobe signal input pin. Read out data at the low level.	
6	DB17	I/O	Data bus	
7	DB16	I/O	Data bus	
8	DB15	I/O	Data bus	
9	DB14	I/O	Data bus	
10	DB13	I/O	Data bus	
11	DB12	I/O	Data bus	
12	DB11	I/O	Data bus	
13	DB10	I/O	Data bus	
14	DB9	I/O	Data bus	
15	DB8	I/O	Data bus	
16	DB7	I/O	Data bus	
17	DB6	I/O	Data bus	
18	DB5	I/O	Data bus	
19	DB4	I/O	Data bus	
20	DB3	I/O	Data bus	
21	DB2	I/O	Data bus	
22	DB1	I/O	Data bus	
23	DB0	I/O	Data bus	
24	/CS	I	Chip select signal input pin (low active).	
25	RS	I	Register select pin. Low: Index/status, High: Control	
26	RESET	I	Reset pin. Initializes the IC when low. Must be reset after power-on.	
27	/WR	I	80-system Write strobe signal input pin. Data is fetched at the "low" level.	
28	VSS	I	System ground.	
29	LED_GND	I	LED Ground	
30	LED_VCC	I	LED Power	
31	NC	-	No connection	

LCD schematic



AC characteristic-18/16 bit 80 system



Conditions (V_{DD3} =2.3V to 3.3V, V_{CI}=2.5V to 3.3V)

Characteristic		Symbol	Specification		Unit
			Min	Max	
Cycle time	Write	tCYCW80	100	-	ns
	Read	tCYCR80	500	-	
Pulse rise / fall time		tR , tF	-	25	
Pulse width low	Write	tWLW80	40	-	
	Read	tWLR80	250	-	
Pulse width high	Write	tWHW80	40	-	
	Read	tWHR80	200	-	
RW , RS and CSB setup time		tAS80	10	-	
RW , RS and CSB hold time		tAH80	2	-	
Write data setup time		tWDS80	60	-	
Write data hold time		tWDH80	15	-	
Read data delay time		tRDD80	-	200	
Read data hold time		tRDH80	5	-	